CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) Competition
Executive Summary

Federal Agency Name:	U.S. Department of Commerce (DOC), National Institute of Standards and Technology (NIST)
Federal Funding Opportunity Title:	FY 2025 CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) Competition Notice of Funding Opportunity (NOFO)
Funding Opportunity Number:	2025-NIST-CHIPS-AIAE-Sustainability-01
Funding Opportunity Description:	Subject to the availability of funds, this NOFO seeks applications for industry-informed, university-based artificial intelligence-powered autonomous experimentation (AI/AE) collaborations, including research and development, education and workforce development, and related activities relevant to sustainable semiconductor materials and processes. If successful, awards made under this NOFO will support the long-term viability of next-generation domestic semiconductor manufacturing, accelerating the discovery, design, synthesis, and adoption of materials and processes, and the development of new researchers needed to meet the industry's technology, economic, and sustainability goals.
Announcement Type:	Initial.
Funding Instrument Type:	Awards under this program will be made as other transaction agreements as authorized, in 15 U.S.C. § 4659(a)(1).
Assistance Listing Number (formerly known as the CFDA Number):	11.042: CHIPS R&D
Award Period of Performance:	Project period of performance up to five (5) years.

Goals and Objectives:

Through awards made under this NOFO, the CHIPS Research and Development Office (CHIPS R&D) aims to achieve the following objectives:

1) Accelerate research into and delivery of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
2) Propagate models for incorporating sustainability metrics into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
3) Expand the capabilities of emerging research institutions and other emerging R&D participants through cohesive, innovative teams of universities, industry, government labs, and other stakeholders; and
4) Build an exceptional workforce of university graduates and faculty with AI/AE R&D expertise.

If successful, CHIPS R&D investments under this NOFO should demonstrate that new sustainable semiconductor materials and processes, meeting industry needs, can be designed and adopted for industry testing within five years. Further, the investment should accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem.

Eligible Applicants and Subrecipients:

Under this NOFO, eligible applicants are domestic accredited institutions of higher education and domestic non-profit or for-profit organizations that manage consortia of accredited institutions of higher education. A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory). Eligible applicants may submit only one concept paper and, if invited, one full application.

Eligible subrecipients under this NOFO include accredited institutions of higher education; for-profit organizations or non-profit organizations; State, local, territorial, and Tribal governments; Federally Funded Research and Development Centers; Federal entities; foreign partners; and other entities eligible to participate

as applicants. Eligible subrecipients may participate in multiple applications.

Vendors selling goods or services in the ordinary course of business are not considered subrecipients under this NOFO.

Available Funding:

CHIPS R&D anticipates that the total Federal funds available under this NOFO to be approximately $100 million.

Cost Share or Match:

Non-federal cost share is not required in this program. However, CHIPS R&D encourages applicants to detail in their applications opportunities for optional co-investment, which may include industry-provided expertise, intellectual property, facility access, or other forms of partner co-investment during the award period of performance. For more information on optional co-investments, see Section 3.2.

Estimated Number of Awards:

Multiple awards in amounts ranging from approximately $20 to $40 million per award in Federal funds, with a period of performance of up to five (5) years, per award are anticipated under this NOFO, for projects varying in scope.

Submission Dates and Times:

Relevant dates in the application process for this NOFO are listed below in Table 1 and described in the text that follows.

Table 1. Key Dates for 2025-NIST-CHIPS-AIAE-Sustainability-01

NOFO Publication Date	October 30, 2024
Informational Webinar	November 8, 2024
Proposers' Day Meeting	November 15, 2024
Concept Papers Due	January 13, 2025, 11:59 PM, 75 days after publication
Invited Full Applications Due	Full application deadlines will be communicated to invited applicants at the time of invitation

	The U.S. Department of Commerce may amend this NOFO at any time. It may also close this funding opportunity with at least 60 days' notice. Any changes will be communicated via https://www.grants.gov and https://www.chips.gov.
How to Apply:	Concept papers and full applications must be submitted electronically through Grants.gov. Paper or emailed submissions will not be accepted. Prospective applicants and subrecipients are required to have an active registration in the System of Award Management (https://sam.gov/content/home) prior to submitting an application and throughout the award term and are encouraged to begin the process of registering as early as possible.
Informational Webinar:	**Informational Webinar:** The National Institute of Standards and Technology (NIST) CHIPS for America Research and Development Office (CHIPS R&D) will host an informational webinar on November 8, 2024, to provide general information regarding this NOFO, offer general guidance on preparing applications, and answer questions. Proprietary technical discussions about specific project ideas will not be permitted during the webinar, and CHIPS R&D staff will not critique or provide feedback on any specific project ideas while they are being developed by an applicant, brought forth during the webinar, or at any time before the deadline for applications. However, questions about this funding opportunity, eligibility requirements, evaluation and award criteria, selection process, and the general characteristics of a competitive application will be addressed during the webinar and by e-mail for inquiries sent to research@chips.gov with "2025-NIST-CHIPS-AIAE-Sustainability-01 Questions" in the subject line. There is no cost to attend the webinar, but participants must register in advance. Participation in the webinar is not required and will not be considered in the review and selection process described in Section 5.5 of this NOFO. **Proposers' Day and Teaming Meetings:** In addition to the informational webinar described above, CHIPS R&D plans to host one or more Proposers' Days to promote awareness of the funding opportunity and

	provide a forum for organizations to identify prospective partners. Information about the event can be found on the CHIPS for America events website.
Application Submission Requirements:	**Concept Papers:** The submission of a concept paper is required. Concept papers will be accepted only through Grants.gov. Concept papers must be received at Grants.gov no later than 11:59 p.m. Eastern Time, on January 13, 2025. Concept papers received after the specified deadline will not be reviewed or considered. Applicants should be aware, and factor into their concept paper submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants should visit Grants.gov for information on any scheduled closures. Please note that an active registration in the System for Award Management is required to submit concept paper materials through Grants.gov. **Full Applications:** Full applications will be accepted only from those applicants that are invited after completion of the concept paper evaluation. Full applications will be accepted only through Grants.gov. The full application deadline will be communicated to invited applicants at the time of invitation. Full applications received after the specified deadline will not be reviewed or considered.
Agency Contacts:	Any inquiries regarding this NOFO must be submitted to the agency points of contact listed in Section 7 of this NOFO. Applicants may submit questions by e-mail to the appropriate agency point of contact with "2025-NIST-CHIPS-AIAE-Sustainability-01" in the subject line. **Programmatic and Technical Questions:** Research@chips.gov **Agreements Rules and Regulations:** Lisa Ko NOFO@nist.gov
Additional Information:	CHIPS R&D has a public website that includes a Frequently Asked Questions page and other information pertaining to this funding opportunity.

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1 PROGRAM DESCRIPTION

The statutory authorities for the CHIPS AI/AE for Rapid, Industry-informed Sustainable Semiconductor Materials and Processes (CARISSMA) program NOFO are 15 U.S.C. § 4656(c) and 15 U.S.C. § 4659, as amended.[a]

1.1 PROGRAM OVERVIEW

The 2022 CHIPS and Science Act appropriated $50 billion to the U.S. Department of Commerce's (the Department or DOC) CHIPS for America program to strengthen semiconductor manufacturing in the United States. This amount includes $39 billion for the Department to onshore semiconductor manufacturing through an incentives program and $11 billion to advance U.S. leadership in semiconductor research and development (R&D). These R&D advances will primarily be realized through the following four programs: the CHIPS National Semiconductor Technology Center (NSTC), the CHIPS National Advanced Packaging Manufacturing Program (NAPMP), the CHIPS Metrology Program, and the CHIPS Manufacturing USA Program (MFG USA). These investments, across both the R&D and incentives programs, seek to strengthen U.S. competitiveness, support domestic production and innovation, create good jobs across the country—with working conditions consistent with the Good Jobs Principles published by the Department of Commerce and the U.S. Department of Labor—and advance U.S. economic and national security.

The CARISSMA program will complement these efforts by generating or enhancing sustainable semiconductor materials and processes. Research outputs should prove relevant and translatable to industry, the NSTC, the CHIPS Manufacturing USA Program, and other CHIPS programs. The competition should further enhance participation in and availability of academic-industry partnerships and research infrastructure for CHIPS Act funded activities and the development of a thriving semiconductor-related AI/AE talent pool.

1.1.1 CHIPS R&D Mission and Goals

Within the CHIPS for America program, the mission of the National Institute of Standards and Technology (NIST) CHIPS Research and Development Office (CHIPS R&D) is to accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities. CHIPS R&D aims to achieve the following goals by 2030:

- ***U.S. Technology Leadership***: The United States improves its capacity to invent, develop, prototype, manufacture, and deploy the foundational semiconductor technologies of the future;

[a] DOC CHIPS activities were authorized by Title XCIX—Creating Helpful Incentives to Produce Semiconductors for America of the William M. (Mac) Thornberry National Defense Authorization Act for Fiscal Year 2021 (Pub. L. 116-283), often referred to as the CHIPS Act, codified at 15 U.S.C. § 4651 et seq., as amended.

- ***Accelerated Ideas to Market***: The best ideas achieve commercial scale as quickly and cost effectively as possible; and
- ***Robust Semiconductor Workforce***: Inventors, designers, researchers, developers, engineers, technicians, and staff sustainably meet evolving domestic government and commercial sector needs.

1.1.2 NOFO Objectives

Accelerated discovery, design, and validation of new materials promises critical benefits to the future of the global semiconductor industry.[b,c,d] These materials must not only yield higher-performing semiconductor products but also address sustainability concerns challenging the industry, including the use of toxic chemicals, greenhouse gas (GHG) emissions, and water and energy efficiency. However, the deployment of new materials and processes can require years of research, development, testing, and validation.

AI/AE has emerged as a potentially game-changing approach to accelerate materials discovery and development. This NOFO therefore aims to create collaborations between academia and the private sector that are university-led, industry-informed, and relevant to sustainable semiconductor manufacturing. These collaborations should support the long-term viability of domestic semiconductor manufacturing by accelerating the discovery, design, synthesis, and deployment of new materials and processes; developing and connecting cutting-edge AI/AE techniques, know-how, and infrastructure; and developing new researchers needed to meet the industry's technological, economic, and sustainability goals.

If successful, CHIPS R&D investments under this NOFO should demonstrate that new sustainable semiconductor materials and processes, meeting industry needs, can be designed and adopted for industry testing within five years. Further, the investment should accelerate a step-change in the number of universities, researchers, and graduates participating in the U.S. semiconductor R&D ecosystem.

The resulting objectives under this NOFO are to:

(1) Accelerate research into and delivery of targeted, industry-relevant, sustainable semiconductor materials and processes through the application of AI/AE;
(2) Propagate models for incorporating sustainability metrics into semiconductor industry materials design and discovery, in addition to continued advancement in power, performance, area, cost, or other relevant technology metrics;
(3) Expand the capabilities of emerging research institutions (ERIs) and other emerging R&D participants through cohesive innovative teams of universities, industry, government labs, and other stakeholders; and

[b] Semiconductor Research Corporation, "MAPT Microelectronics and Advanced Packaging Technologies Roadmap", 2023. Available online at: srcmapt.org/wp-content/uploads/2024/03/SRC-MAPT-Roadmap-2023-v4.pdf
[c] AI Aspirations: AI for Sustainable Materials, White House Office of Science and Technology Policy, 2024. Available online at: ai.gov/aspirations/
[d] National Strategy on Microelectronics Research, A Report by the Subcommittee on Microelectronics Leadership, March 2024. Available online at https://www.whitehouse.gov/wp-content/uploads/2024/03/National-Strategy-on-Microelectronics-Research-March-2024.pdf

(4) Build an exceptional workforce of university graduates and faculty with AI/AE R&D expertise.

The anticipated program outcomes, if successful, should prove relevant and translatable to the NSTC, the CHIPS Manufacturing USA Institute, and other CHIPS programs.

1.2 DEFINITIONS

For purposes of this NOFO, the terms listed below shall have the following meanings:

(1) **Applied Research** – "Original investigation undertaken in order to acquire new knowledge. Applied research is, however, directed primarily towards a specific practical aim or objective."[1]

(2) **AI-enabled autonomous experimentation (AI/AE)** – The combination of automated (robotic) hardware for materials synthesis and characterization, AI-powered software and models, and data acquisition, analysis, computational resources, and storage hardware that plan, execute, and evaluate experiments in autonomous closed loops to achieve accelerated research objectives supplied by human researchers.[2]

(3) **Basic Research** – "Experimental or theoretical work undertaken primarily to acquire new knowledge of the underlying foundations of phenomena and observable facts. Basic research may include activities with broad or general applications in mind, such as the study of how plant genomes change, but should exclude research directed towards a specific application or requirement, such as the optimization of the genome of a specific crop species."[3]

(4) **Digital Twin** – A set of virtual information constructs that mimics the structure, context, and behavior of a natural, engineered, or social system (or system-of-systems). Typically, a digital twin can be dynamically updated with data from its physical twin, has a predictive capability, and informs decisions that realize value.[4]

(5) **Emerging Research Institution or ERI** – An institution of higher education with an established undergraduate or graduate program that conducts less than $50,000,000 per year in Federal research expenditures.[5] The Department of Energy maintains an online list of Institution Designations, including ERIs.

(6) **Materials Digital Twin** – Either (i) a model of the performance of material in response to changes in its environment, or (ii) a model of the synthesis of a material, and its response to changes in synthesis control variables.

(7) **Milestones** – Actions or events marking a significant change or stage in developments in a project.

(8) **Phase-specific Target** – Derived from applicant-specified SMART Milestones, phase-specific targets inform go/revise/no-go points for the transition from one project phase to the next. Phase-specific targets may address measurable progress toward either Co-optimization Targets, Programmatic Targets, or both.

(9) **Project** – All activities funded under a single award made under this NOFO, including but not limited to all planning and management; basic and applied research; the development and production of manufactured materials and devices, systems, equipment, tools, and software, as appropriate to the funded work; preparation for

commercial viability and domestic production of funded innovations; and education and workforce development activities.

(10) **Project Team** – Any funded entity (the applicant and any proposed subrecipients), as well as unfunded collaborators planned for inclusion in a single proposal under this NOFO.

(11) **Recipient** – The entity that receives an award directly from a Federal awarding agency to carry out an activity under a financial assistance program.

(12) **Research Outputs** – The results of research funded under this NOFO, including but not limited to data, models, materials, and processes, such as materials property datasets; predictive algorithms; physically manufactured prototype materials; materials digital twins; and manufacturing sustainability design guidelines and frameworks.

(13) **Semiconductor** – An integrated electronic device or system, most commonly manufactured using materials such as, but not limited to, silicon, silicon carbide, or III-V compounds, and processes such as, but not limited to, lithography, deposition, and etching. Such devices and systems include but are not limited to analog and digital electronics, power electronics, and photonics, for memory, processing, sensing, actuation, and communications applications.

(14) **Semiconductor manufacturing** – All activities encompassed by the semiconductor fabrication, advanced packaging, assembly, and test processes, including but not limited to wafer manufacturing.

(15) **Semiconductor materials** – The broad class of materials contained in semiconductor devices and systems (see "semiconductor" definition) as the result of semiconductor manufacturing (which includes packaging), including materials used in semiconductor manufacturing that do not remain in the final product.

(16) **SMART** – A framework for writing objectives that are Specific, Measurable, Achievable, Relevant, and Time-Bound and provide the details for how an organization will achieve an objective.

(17) **Subrecipient** – An entity that is eligible to receive a subaward from a Recipient to carry out activities under an award made under this NOFO, such as research and development activities, education and workforce efforts, and other integral project activities. Vendors selling goods or services in the ordinary course of business are not considered subrecipients for purposes of this NOFO.

(18) **Sustainability / Sustainable** – The ability to meet the needs of the present without compromising the ability of future generations to meet their own needs. Sustainability has three primary goals: (1) protecting the environment, (2) protecting human health and safety of individuals and communities, and (3) promoting economic prosperity and economic objectives.[6]

1.3 BACKGROUND

In its 2023 Microelectronics and Advanced Packaging Technologies Roadmap, the Semiconductor Research Corporation reported on the demand for innovative, sustainable semiconductor materials and chemistries for current and next generation semiconductors and semiconductor manufacturing. The Roadmap noted that "tools encompassing co-optimization of performance metrics and environmental, health, and safety metrics will help accelerate the

discovery of more sustainable materials and chemicals without compromising the performance of the product."[7] Other industry reports, including reports published by the Semiconductor PFAS[e] Consortium, recognize the need for innovation in sustainable materials.[8] These include identifying safer alternatives to existing semiconductor manufacturing materials to developing more effective abatement technologies that prevent the release of chemicals that are harmful to the environment and human health.[9] As the United States and other nations invest in semiconductor manufacturing, these reports reflect a need for manufacturing and its resulting products to demonstrate both high performance and sustainability. While AI/AE provides an opportunity to address these dual objectives, the industry must nonetheless tackle co-existing challenges:

(1) economic pressure to address sustainability;
(2) difficulty optimizing across sustainability and performance metrics at the accelerated timelines necessary for impact and competitive edge; and
(3) the limited AI/AE infrastructure and workforce.

1.3.1 Challenge: Economic Pressure

Semiconductor manufacturing requires significant amounts of both water and energy, while using chemicals considered harmful to human health, if released. Examples are as follows:

- The average chip fabrication plant uses 10 million gallons of ultrapure water every day[10, 11], the equivalent of 33,000 U.S. homes' consumption;[12]
- Depending on the plant, electricity consumption represents between 5% and 30% of its operating costs, totaling $20-$30 million per year. A typical semiconductor plant uses as much energy in a year as about 50,000 homes;[13] and
- In 2022, the electronics manufacturing industry was responsible for 5 million metric tons of CO_2-equivalent emissions from fluorinated gases.[14]

Given the environmental impact of the semiconductor fabrication process, regulators, manufacturers, and customers have sought more sustainable practices and solutions, including to reduce manufacturing and operating costs as well as litigation and supply chain risks. For instance,

- Prominent semiconductor companies have targeted water reuse/restore/recycle of up to 75% or reductions in water usage reductions by up to 33%;[15]
- At least three manufacturers have announced significant energy consumption reduction, including targets for energy per unit produced, as well significant GHG reduction targets;[16,17,18] and
- One major PFAS supplier is planning to exit the market due to shifting liability. [19] Another PFAS supplier has pledged to phase out certain PFAS related products and processes.[20] Regulatory concerns have raised supply chain risks, with no known alternatives currently existing for many PFAS-containing materials used in the semiconductor industry.[21]

[e] Perfluoroalkyl and polyfluoroalkyl substances.

When considering the full product lifecycle, semiconductor products prove even more energy-intensive with high environmental impacts. For instance, U.S. data centers comprise roughly 2% of total U.S. electricity usage, according to the Department of Energy.[22]

1.3.2 Challenge: Materials Co-optimization and Time to Deployment

Traditional methods for discovery and deployment of new semiconductor materials—with a focus on improving semiconductor performance while decreasing power usage, physical area, and cost—can require years, even decades, of research, development, testing and validation before deployment.[23] Material characterization experiments, which validate and inform models, are time and labor intensive and often the rate-limiting step in a material validation campaign. Moreover, a lack of validating experiments limits current models of materials design. Including materials sustainability will likely increase these challenges; limit the material candidate pool due to some candidates' toxicity, effects on human health, and environmental impact; and increase the time required for materials discovery and validation. By way of example, when considering the potential for PFAS replacements to impact multiple parts of the precisely-calibrated semiconductor supply chain, the Semiconductor Industry Association (SIA) concluded that timelines for adoption of non-PFAS materials adoption can range from—

- 3 to 4 years, if there is an existing non-PFAS alternative available that can be demonstrated to provide adequate performance for a specific application;
- 3 to 15 years, where existing non-PFAS alternative may be viable but require tooling and/or process changes; and
- Up to 25 years for new chemicals or the development of alternative approaches to manufacturing devices.[24]

1.3.3 Challenge: Limited Research Workforce

In its recent workshop report on AI/AE, an Interagency Working Group of the Materials Genome Initiative (MGI) found an essential role for researchers in "supporting industrial development and aligning fundamental research with broader industry goals, such as carbon neutrality and manufacturability."[25] The Working Group's report further highlighted a demand for graduates trained in autonomous experimentation and materials R&D, with "the combination of AI/ML coding skills and the specific specialization in their respective materials field."[26]

However, the same report estimated that the United States had few institutions ready to conduct fully autonomous AI/AE research in electronics and photonics materials, much less research relevant to semiconductor materials sustainability. This presents a challenge for acquiring the needed research staff, particularly given SIA's projection of 27,300 semiconductor industry engineering roles remaining unfilled due to an insufficient number of graduates in relevant technical fields. These include 9,900 bachelor's, 12,300 master's, and 5,100 PhD-level graduates, in addition to 13,400 computer scientists.[27] A similar assessment by the Department of Commerce Bureau of Industry and Security indicates that the expansion of the semiconductor workforce will require an estimated 54,000 new jobs requiring four-year degrees and 16,000 new jobs not requiring a four-year degree.[28] Given these considerations, the MGI Working Group

specifically identified building the workforce, particularly the U.S. citizen workforce, as a key area for action.

1.3.4 Opportunity: AI/AE

Through efforts such as the MGI, the United States has made significant investments into discovering new materials for a range of industries and applications. Recent technological advances, including the rapid improvements in artificial intelligence, suggest an opportunity to more efficiently explore the real-world properties of these and other materials. For instance—

- A major U.S. company leveraged AI/AE to analyze 6,000 data sources to generate 3,000 replacement candidates for potentially toxic semiconductor materials, demonstrating a 100-fold reduction in candidates tested compared to a human toxicologist;[29]
- The Defense Advanced Research Agency (DARPA) funded a multi-location self-driving lab to identify 21 promising materials from a set of 150k+ candidates over two months;[30] and
- A U.S. Department of Energy (DOE) National Lab used AI/AE to synthesize 41 of 58 target compounds over 17 days.[31]

As demonstrated by the efforts described above, AI/AE has a significant advantage over traditional materials R&D methods in allowing researchers to rapidly explore a vast set of design and manufacturing parameters and develop models for their optimization. With direct and continuous contribution from industry on material properties, process requirements, reliability and compatibility, supply chain and cost, and/or lifecycle analysis for sustainability, AI/AE opens a much richer parameter space for co-optimization and should accelerate the time from design to production.

1.3.5 Opportunity: Emerging Research Institutions

Multiple Federal laws and policies direct NIST to address shortages in the semiconductor workforce and to increase participation in semiconductor R&D, including by "establishing a dynamic, collaborative network for microelectronics research", "[supporting] a broad range of stakeholders and communities", and "[investing in] workforce development, basic and translational research, and related infrastructure."[f] Emerging Research Institutions provide a unique opportunity to meet this directive while addressing the lack of researchers participating in AI/AE. Per a 2009 National Academies workshop report on ERIs, providing research experiences to students can help increase student retention and employment in the related field, increase the likelihood that students seek graduate education, and improve the participation of underrepresented groups.[32] However, while ERIs serve the majority of students in STEM fields, they receive only 10% of Federal funding for R&D in science and engineering.[33] Increasing ERI research capacity therefore represents an available resource for addressing limitations not only in the amount of experimental data available for AI/AE, but also in the AI/AE and broader semiconductor workforce. Given that it is a relatively new field, one that generally involves the transfer of digital products, and can support distributed research models, AI/AE may be uniquely

[f] Executive Order 14080—Implementation of the CHIPS Act of 2022

suited to partnerships between ERIs and leading institutions, with ERIs helping to provide both the data and researchers needed to grow the field.

1.4 FUNDING OPPORTUNITY DETAILED DESCRIPTION

Consistent with the objectives listed in Section 1.1.2, responsive applications to this NOFO must propose establishing a collaboration among one or more semiconductor industry companies, research universities or national laboratories with demonstrated experience in AI/AE or in related fields, and at least one ERI (or a domestic non-profit or for-profit organization that manage a consortium of ERIs). The National Cooperative Research and Production Act of 1993, as amended (codified at 15 U.S.C. § 4301 et seq.), addresses awardee "joint ventures" (as defined therein) for research and development funded under this award.

Further, consistent with the direction under Executive Order 14080 (Implementation of the CHIPS Act of 2022), CHIPS R&D encourages that proposals include recipients or subrecipients such that awards significantly expand the capabilities of emerging research institutions in partnership with industry, other research universities, and national laboratories.

In order to achieve the objectives of this NOFO, CHIPS encourages and will favorably consider applications that demonstrate strong industry participation in the development of and execution of the funded research. CHIPS R&D further encourages participation by civil society or labor organizations focused on environmental sustainability or human health and safety, where appropriate. Specific project activities are expected to include but not necessarily be limited to:

(1) establishing the collaboration;
(2) refining Co-optimization and Programmatic Targets (see Sections 1.4.3 and 1.4.4) relevant to a chosen set of materials classes and applications (see Section 1.4.2);
(3) conducting basic and applied research guided by the targets;
(4) training students and faculty; and
(5) transitioning developed technologies to higher technology readiness levels (TRLs).

1.4.1 Operational Areas

Responsive applications to this NOFO must propose activities, milestones, and deliverables to address the following three Operational Areas (OAs):

(1) **OA1: Convening, Roadmapping, and Technology Transfer**: Establishing lasting collaborations between stakeholders, refining Co-optimization and Programmatic Targets, and transferring research outputs for further use.
(2) **OA2: AI/AE Infrastructure and Research**: Establishing AI/AE capabilities, to include infrastructure at ERIs and other research universities or access to such infrastructure, and conducting basic and applied research into early TRL materials and processes that address semiconductor industry needs.
(3) **OA3: Education and Workforce Development**: Developing and expanding the total number of domestic researchers skilled in AI/AE methods relevant to the semiconductor industry materials and processes.

1.4.2 Materials Classes and Applications

Consistent with the objectives listed in Section 1.1.2, responsive applications to this NOFO must propose focusing project activities on specific material classes and applications relevant to semiconductor manufacturing. Proposals must demonstrate the expected impact on metrics related to both the sustainability of semiconductor manufacturing and to materials, process, or device performance characteristics, which may include device performance, power, area, and cost (PPAC). Proposals may seek to either improve existing materials and processes or enable realization of next-generation materials, processes, or devices.

To support an understanding of the desired approach, Table 2 below provides notional, non-exhaustive examples of materials classes and applications relevant to semiconductor manufacturing. Such examples include:

- ***PFAS Alternatives.*** Developing and improving the performance of PFAS replacements for use in multiple applications (e.g., photoresists, antireflective coatings, heat transfer fluids, and advanced packaging materials), reducing manufacturing PFAS emissions.
- ***Next-Generation Photoresist.*** Developing photoresist materials (e.g., resins, solvents, photoactive compounds, etc.), to enable next-generation process nodes while reducing fab energy consumption and emissions.
- ***Materials for Improved Device Heat Transfer.*** Developing PFAS-free, higher performance thermal interface materials, high conductivity materials, and heat transfer materials for immersion and liquid cooling, to improve the power efficiency of data centers while reducing PFAS emissions throughout the supply chain.

Table 2. Non-Exhaustive List of Notional Materials Classes and Applications

• Abatement catalysts • Adhesives • Atomic Layer Deposition (ALD) • Antireflective Coatings • Chemical Mechanical Planarization (CMP) slurries • Dielectrics and insulators • Dopants • Epitaxy and deposition gases • Etch gases • Filters and membranes • Heat transfer fluids (HTFs) • Interconnects • Lubricants	• Memory materials • Metals and conductors • PFAS • Polymers and resins • Photonic materials • Photoresists • Photoacid generators (PAGs) • Redistribution Layer films (RDLs) • Solvents • Substrates • Surfactants • Thermal Interface Materials (TIMs) • Underfills • Wet etchants • 2D materials

1.4.3 Co-optimization Targets

Responsive applications to this NOFO must propose to pursue—through basic and applied research and the development of analytic models—targeted, industry-relevant materials and processes that co-optimize power- and performance-related materials, process, or device characteristics (see Theme 1 below) and sustainability targets (see Themes 2 – 4 below). Co-optimization Targets that address the environmental impacts of semiconductors over their lifecycle, such as the total power consumed by a device, may be considered within Theme 1. **Applications that pursue manufacturing sustainability (Themes 2 – 4) without co-optimizing for Theme 1 will be considered out of scope.**

Proposals must address at least one or more of Themes 2, 3, or 4, to target improvements in the sustainability of current or future semiconductor manufacturing techniques. **Proposals that improve device performance without addressing manufacturing sustainability will be considered out of scope.** CHIPS R&D may prioritize applications that credibly address sustainability targets across multiple themes.

1.4.3.1 Theme 1: Materials, Process, or Device Power- and Performance- related Characteristics

Responsive applications to this NOFO must propose Co-optimization Targets based on industry-relevant materials, process, or device power- and performance-related characteristics, which may include PPAC and other related metrics such as yield, economic metrics, and supply chain resiliency metrics. As a notional example, Theme 1 Co-optimization Targets relevant to photoacid generator (PAG) performance and cost criteria include acid strength, acid diffusivity, pattern quality, solubility in casting solvents, manufacturing cost, and processing temperature.[34] More advanced models or digital twins could further consider how changing PAG characteristics might impact downstream process and device performance (including PPAC), via factors such as area scaling or semiconductor design complexity. Conversely, PAG sustainability targets (Themes 2 – 4) may include toxicity and environmental persistence.

CHIPS R&D expects that, in identifying Co-optimization Targets, applications will aim to develop materials and processes that result in similar or improved materials, process, and/or device characteristics compared to currently known materials and processes. If such characteristics do not constitute an improvement over the state of the art or state of the practice, applicants must demonstrate the industry-relevance of the proposal, such as through stakeholder Letters of Commitment/Interest.

1.4.3.2 Theme 2: Emissions and Hazardous Waste

Applications that address Theme 2 must propose Co-optimization Targets that demonstrate improvement related to GHG emissions, use of toxic substances, and generation of hazardous waste from current or future semiconductor manufacturing. Sample targets may include but are not limited to, for instance, the mass or volume of a substance (e.g., GHGs or PFAS) released into the environment per 300mm wafer manufactured. Applicants may further propose to address targets related to the toxicity or human health and safety impact of semiconductor manufacturing-related emissions or hazardous waste.

1.4.3.3 Theme 3: Energy Consumption

Applications that address Theme 3 must propose Co-optimization Targets that demonstrate improvement related to the amount of energy consumed by current or future semiconductor manufacturing. Sample target may include but are not limited to, for instance, kilowatt hours (kWh) per 300mm wafer manufactured. Manufacturing energy consumption differs from the amount of power (energy) consumed by a manufactured device, circuit, or system, which would be considered as a potential Theme 1 Co-optimization Target.

1.4.3.4 Theme 4: Water Consumption

Applications that address Theme 4 must propose Co-optimization Targets that demonstrate improvement related to water consumed by current or future semiconductor manufacturing. Targets may include, but are not limited to, targets related to amount of fresh water consumed from public utilities as well as targets related to recycling or reclamation of used process water. Sample targets may include but are not limited to, for instance, gallons of water used per 300mm wafer manufactured.

1.4.4 Programmatic Targets

Responsive applications to this NOFO must propose to pursue improvements in the domestic capabilities for AI/AE research (Theme 5) and in the research-trained semiconductor workforce (Theme 6). Responsive applications must further propose to pursue the domestic transfer of CHIPS-funded technologies (Theme 7).

1.4.4.1 Theme 5: Research Capacity

Applications must propose Programmatic Targets that demonstrate how CHIPS-funded activities will increase the overall research capacity of the domestic semiconductor innovation ecosystem, particularly as it relates to AI/AE. Sample targets may include but are not limited to, for instance:

(1) the number of faculty able to substantively engage in relevant research, including after the period of performance;
(2) the administrative and physical infrastructure (e.g., equipment) available for performing AI/AE research in sustainable semiconductor materials at funded institutions, including through co-investment;
(3) the long-term availability, both to universities and industry, of physical and digital infrastructure for AI/AE research; and
(4) the overall research productivity of funded institutions (e.g., publication activity, patent activity, or research expenditures) in semiconductor-related fields, and
(5) partnerships with entities focused on innovation, entrepreneurship, access to capital, and technology commercialization.

Applications must specify the distribution of increased research capacity between ERIs and non-ERIs. CHIPS R&D will favorably consider applications that demonstrate a substantial increase in research capacity and research leadership at ERIs.

1.4.4.2 Theme 6: Education and Workforce Development

Applications must provide an **Education and Workforce Development (EWD) Plan** with Programmatic Targets that represent improvements in the availability of state-of-the-art (SOTA) research-trained personnel. Sample targets may include but are not limited to, for instance, improvements in:

(1) the number of undergraduate, masters, or doctoral students provided significant research experiences (e.g., paid research internships and fellowships) and direct mentorship by industry or other private sector partners in semiconductor-relevant AI/AE research;
(2) the number of relevant industry and other private sector roles within educational institutions (e.g., visiting scientists, adjunct faculty, and research fellows),
(3) access to semiconductor or AI/AE relevant training at the partner educational institutions; and
(4) the number of graduating students that enter the domestic semiconductor workforce in manufacturing, design, and R&D.

Applications must specify the distribution of EWD improvements between ERIs and non-ERIs. CHIPS R&D will favorably consider applications that demonstrate substantial EWD improvements at ERIs.

1.4.4.3 Theme 7: Domestic Technology Transfer

Applications must propose Programmatic Targets that demonstrate, with rigor increasing across the award period of performance, the ability for CHIPS-funded research outputs to successfully transfer to the domestic commercial marketplace. CHIPS R&D strongly encourages applicants to work with industry partners when developing these targets and to ensure consistency with the **Commercial Viability and Domestic Production Plan (CVDP)** as discussed in Section 2.6.4 of this NOFO. Sample targets may include but are not limited to, for instance:

(1) the number and quality of industry partnerships, including through a Research Advisory Board (RAB);
(2) direct participation of industry in research funded under this award;
(3) participation of funded institutions in the CHIPS Manufacturing USA Institute;
(4) patenting and licensing activities, or other evidence indicating the adoption of funded research outputs by domestic partners or by CHIPS-funded programs;
(5) measures of alignment with industry needs, as demonstrated through technoeconomic analyses, relevant co-investment, or other means; and
(6) the number and quality of research outputs transitioned to industry for testing or integration into co-optimization models or pilot lines, where appropriate.

Applicants should be aware that the CVDP represents an initial assessment of the commercial viability and domestic production opportunities of potential funded research outputs, with

updates occurring across the award period. Given this NOFO's focus on industry-informed, university-based collaborations, CHIPS R&D anticipates that Phase 1 Theme 7 targets may largely focus on strengthening industry partnerships, conducting technoeconomic analyses, and informing the CVDP. CHIPS R&D expects that awardees will refine more definitive applicant-proposed metrics for technology transfer during Phase 1, for tracking during Phases 2 and 3.

1.4.5 Phases of Work and SMART Milestones

Responsive applications to this NOFO must propose three phases of work, with the first phase ranging from 12 to 18 months and each subsequent phase ranging in length from 12 to 24 months. The total period of performance may not exceed five (5) years.

Responsive applications to this NOFO must further define, for each OA and within each phase, SMART Milestones marking measurable progress towards demonstrating the Co-optimization Targets (Section 1.4.3) and achieving the Programmatic Targets (Section 1.4.4).

In coordination with NIST's Financial Assistance Agreements Management Office (FAAMO), CHIPS R&D may conduct negotiations with applicants deemed meritorious by the evaluation panel and determined by CHIPS R&D to stand a reasonable chance of being funded, in order to (1) refine the proposed milestones (2) define phase-specific targets derived from the proposed milestones, and (3) address other matters as determined by CHIPS R&D. These phase-specific targets will inform go/revise/no-go points for the transition from one project phase to the next.

Upon approval and selection of an application under this NOFO, CHIPS R&D intends to award funding for Phase 1 activities across all Operational Areas, with subsequent phases being considered for funding incrementally. CHIPS R&D retains sole discretion to determine whether a recipient has met the requirements for each Co-optimization Target, Programmatic Target, Phase-specific target, milestone, and deliverable.

Based on the results of CHIPS R&D assessments of research outputs, evaluation of overall progress, availability of funding, and continued alignment with CHIPS R&D priorities, CHIPS R&D, at its sole discretion, will decide at the end of each phase to proceed with the next increment of funding, request a revised plan from the recipient (subject to both the constraints of the approved award scope and budget, and subject to CHIPS R&D approval), or terminate funding for the project.

Figure 1 below shows a hypothetical project timeline with three phases of 18 months, 18 months, and 24 months, with corresponding milestones.

- Finalize teaming structure, including for industry and civil society partner organizations
- Establish Research Advisory Board
- Refine Co-optimization and Programmatic Targets based on technoeconomic and lifecycle analyses
- Refine the Phase-specific Research Plan and CV, including a roadmap from R&D to industry adoption
- Determine AI/AE system components and workflow design
- Install, integrate, and test equipment and software
- Assemble project team with faculty, staff, students, and post-docs onboarded
- Refine EWD Plan and begin to develop and teach AI/AE curricula at participating universities
- Join CHIPS Manufacturing USA Institute and the NSTC, as appropriate

- Continue to conduct basic and applied research based on Phase 1 results
- Demonstrate effective industry-university feedback loops with progress toward targets
- Demonstrate an effective collaboration environment, workflow, throughput, and quality of R&D output of AI/AE systems
- Refine digital twins, custom software, application programming interfaces (APIs), and co-optimization algorithms
- Deploy preliminary materials digital twins
- Deliver first-round materials to industry for assessment with respect to Co-optimization Targets and AI/AE system performance
- Update EWD plan and continue to train students and post-docs using relevant AI/AE curricula

- Conduct tests, led by industry, to establish the performance of multiple co-optimized sustainable semiconductor materials and processes
- Catalog and accelerate technology transfer and adoption by industry partners and secure industry commitments to deploy the technology
- Affirm the commercial viability, environmental impact, and supply chain impacts of potential research outputs
- Disseminate equipment and materials digital twins to industry, the CHIPS Manufacturing USA Institute, and the NSTC, as appropriate
- Execute plans to ensure sustained leadership, capabilities, and capacity for AI/AE at universities, including ERIs, and in the private sector
- Deliver final reports and best practice at CHIPS R&D

1.4.6 Project Team Capabilities and Structure

AI/AE couples automated experimentation (robotically controlled experiments), in situ or inline analysis of experimental results, and the use of artificial intelligence as a decision engine to direct experiments in rapid, closed loops. In responding to this NOFO, CHIPS R&D encourages applicants to consider existing best practices for using artificial intelligence and for AI/AE, including incorporating the major components of an AI/AE system described below. Responsive applications may also consider the role of federated architectures and must include a physical infrastructure and faculty development plan.

1.4.6.1 Major Components of an AI/AE System

AI/AE allows for rapid exploration of the material/process design space, allowing for co-optimization across a vast array of design criteria. Drawing on a 2024 MGI workshop report,[35] elements of an AI/AE system include:

(1) Automation, enabling robots to carry out the experimental tasks such as materials synthesis and preparation, prescribed by the decision algorithms or planners (see point (4) below);
(2) Rapid/automatic characterization of materials to determine their properties, enabled by AI-trained pattern recognition;
(3) Automated data storage and analysis, through well-defined, human-free workflows or pipelines; and

(4) Based on the results of characterization and data analysis, decision algorithms or planners (like Bayesian optimization) to enable tradeoffs between exploration and goal-seeking behavior in the search for desired performance characteristics.

Additionally, CHIPS R&D encourages researchers using AI/AE systems to:

(1) Specify the parameters and desired weights used in the various optimizations (that is, tradeoffs);
(2) Assess the progress of the AI/AE systems and, where necessary, modify the behavior of the system through hardware and software improvements;
(3) Analyze the resulting experimental outputs across a broad range of parameters (such as, for example, environmental toxicity and continued industry relevance) to determine whether a new R&D campaign should be designed;
(4) Assess input data and models to identify any inherent limitations and impact to the performance of the AI/AE system;
(5) Incorporate relevant elements of the voluntary NIST AI Risk Management Framework, such as:
    a. Conducting appropriate diligence on training data and models to avoid possible infringement of a third party's intellectual property or other risks related to privacy, bias, or security;
    b. Incorporating trustworthiness considerations into the design, development, use, and evaluation of AI products, services, and systems; and
    c. Establishing mechanisms to ensure the auditability of the AI system and the explainability of its results, such as documenting the sources of training data.
(6) Incorporate into their **Research Security Plan** a summary of known, intended cybersecurity practices.

1.4.6.2 Federated AI/AE Systems

Significant federation of the digital and physical infrastructure of an AI/AE system is both possible and potentially desirable. Given that much of AI/AE involves the use and transmission of digital objects (e.g., computer code, digital twins, data, and control software enabling remote operation), AI/AE researchers can virtualize pieces of the workflow. Additionally, a "multi-agent" approach, which combines information from diverse research campaigns, can support AI/AE research strategies, including work funded by this NOFO.[36]

1.4.6.3 Physical Infrastructure Plan

In responding to this NOFO, applicants must include a **Physical Infrastructure Plan** that seeks to identify models and tools that must be acquired, developed, deployed, or accessed, such as:

(1) Initial physics/chemistry-based models, AI methods, and other data to feed into the closed loop AI/AE system;
(2) Materials synthesis and characterization equipment;
(3) Robotics and other automation infrastructure and experimental hardware;
(4) Supporting computer software and hardware, including data storage systems; and
(5) Algorithms and data planning tools, including the optimization/planner algorithms.

Given that all elements of the AI/AE system need not be located at a single site, the **Physical Infrastructure Plan** must, consistent with the Relevance to Economic and National Security evaluation criteria, describe the development of long-lasting experimental infrastructure and expertise at multiple institutions. Further, the Plan should ensure that participant institutions, including ERIs, can conduct additional AI/AE campaigns after the completion of this project, yielding a lasting legacy of enhanced domestic AI/AE research capacity. Applicants may propose different models for achieving this requirement while meeting their unique infrastructural needs. Such models may vary from more centralized research "hubs" to a fully federated infrastructure. Where applicable, CHIPS R&D encourages models that allow participating collaborators to remotely access equipment hosted by collaborators from other institutions. Other creative models for sharing digital information between collaborating team members and enabling federated research workflows are also encouraged.

1.4.6.4 Faculty Development

Consistent with the objectives listed in Section 1.1.2, applicants must include a **Project Team Description** and **Faculty Development Plan** that provides for the development of AI/AE-capable faculty involved in research at multiple institutions. The **Project Team Description** must include faculty from one or more ERIs serving as a Principal Investigator or co-Principal Investigator relevant to OA2.

1.5 OA-SPECIFIC ACTIVITIES AND DELIVERABLES

The following subsections provide information specific to each OA, to assist applicants in preparing responsive concept papers (see Section 4.5) and full applications (see Section 4.6). Proposals must address each Operational Area and identify, for each OA and within each phase, SMART milestones marking measurable progress towards multiple Co-optimization Targets (see Section 1.4.3) and Programmatic Targets (see Section 1.4.4).

1.5.1 OA1: Convening, Roadmapping, and Technology Transfer

CHIPS R&D seeks to accelerate the deployment and adoption of industry-relevant sustainable materials and processes into semiconductor manufacturing, propagate models for incorporating sustainability metrics into materials discovery, and expand the capabilities of emerging R&D participants. To achieve these objectives and to ensure that funded research addresses industry-relevant materials needs and challenges, CHIPS R&D expects successful applicants to demonstrate strong partnerships among:

(1) semiconductor industry companies;
(2) one or more Emerging Research Institutions;
(3) other research institutions, including national labs, with demonstrated capabilities in AI/AE or related fields; and
(4) where appropriate, civil society or labor organizations focused on environmental sustainability and human health and safety.

To demonstrate capabilities relevant to OA1, full applications must include an initial **Impact Statement** and **Stakeholder Collaboration Strategy**, including a **CVDP** and **Intellectual Property Rights Management Plan (IPRM)** (see Sections 4.5.1 and 4.6.1).

1.5.1.1 Activities

Teams must further demonstrate a commitment to transitioning research outputs to higher TRL levels. Beginning in Phase 1, CHIPS R&D expects activities under OA1 to include:

(1) Establishing a Research Advisory Board or similar mechanism for the recipient awardee to receive regular guidance on materials challenges and Co-optimization Targets relevant to industry challenges and to sustainability;
(2) Organizing stakeholder liaison meetings, stakeholder engagement days, site visits, or other such activities;
(3) Developing and executing collaboration agreements between industry, research, and civil society partners, which may include opportunities for data exchange, sample sharing, equipment usage, or other productive methods of collaboration;
(4) Conducting technoeconomic and lifecycle analyses to further affirm the commercial viability of potential research outputs as well as environmental impacts of adoption;
(5) Refining or developing new Co-optimization Targets, in coordination with industry and other stakeholders, to guide basic and applied research activities;
(6) Participating in the CHIPS Manufacturing USA Institute and NSTC as appropriate, such as through data sharing, model sharing, virtual prototyping, joint projects, standards development, technical exchanges, training, and workforce development; and
(7) Transferring appropriate research outputs (e.g., data, models, materials and processes) to industry, other private sector stakeholders, the CHIPS Manufacturing USA Institute, NSTC, or other CHIPS-funded programs for further physical and digital validation, advancement to higher TRLs, adoption, and use.

CHIPS R&D strongly recommends applicants to establish a Research Advisory Board, consisting of recognized leaders in the fields of AI/AE, semiconductor manufacturing, and sustainability, to help the recipient awardee evaluate progress and to guide research directions.

1.5.1.2 Deliverables by Phase

OA1 Phase 1 deliverables must include, at a minimum, one or more submissions of:

(1) An updated, stakeholder-informed **Impact Statement**, detailing any refinements in the Materials Classes and Applications, Co-optimization Targets, and Programmatic Targets.
(2) Finalized copies of the **Stakeholder Collaboration Strategy** and any relevant collaboration agreements, including—
    a. agreements operationalizing the IPRM, to include any requirements relevant to ownership and access to training data, trained and untrained models, and research outputs;

b. agreements operationalizing the Research Advisory Board, or similar mechanisms, to receive private sector guidance on research targets;
c. agreements operationalizing other industry partnerships in the funded research; and
d. evidence of participation in the CHIPS Manufacturing USA Institute.

(3) An updated, stakeholder-informed **CVDP**.

OA1 Phase 2 and Phase 3 deliverables must include at a minimum, one or more submissions of:

(1) Updates to the **Impact Statement**, as necessary.
(2) Updates to and progress against the **CVDP**, including information from any relevant technoeconomic and lifecycle analyses.
(3) A **Technology Transition Report**, detailing successful research transitions or technology adoptions, including demonstrated technology transfer to industry partners, the CHIPS Manufacturing USA Institute, the NSTC, or to other CHIPS-funded programs.

1.5.2 OA2: AI/AE Infrastructure and Research

CHIPS R&D seeks to expand the availability of university-based labs capable of performing AI/AE research and to generate research outputs relevant to discovering, designing, validating, and transitioning sustainable materials and processes for next generation semiconductors. Successful AI/AE labs should possess or have access to multiple capabilities, as described in Section 1.4.6 Successful proposals should also develop and transition to further development or broader use new AI/AE models, sustainable materials and processes, and digital twins.

To demonstrate capabilities relevant to OA2, full applications must include an initial **Research and Infrastructure Strategy**, including a **Physical Infrastructure Plan** and **Faculty Development Plan** consistent with Section 1.4.6.

1.5.2.1 Activities

CHIPS R&D expects activities under OA2 to include:

(1) Purchasing, installing, and maintaining necessary equipment including but not limited to synthesis equipment, analytical equipment, robotics/automation, computational resources, and information technology;
(2) Acquiring access to additional equipment, including cyberinfrastructure and computational capabilities, as necessary;
(3) Identify and acquire training data and models, consistent with the requirements of the IPRM (see Section 4.6.1.6);
(4) Hiring and managing necessary research staff including but not limited to faculty, technicians, and students;
(5) Operating a lab, including but not limited to managing budgets, training users, providing technical support to researchers, and the development and execution of AI systems in accordance with established best practices (see Section 1.4.6);
(6) Developing analytic models for incorporating sustainability related metrics into AI/AE materials optimization and updating these models with research findings;

(7) Conducting basic and applied research to discover and validate new materials and processes, relevant to the Co-optimization Targets;
(8) Conducting technoeconomic and lifecycle analyses of discovered materials and processes to assess their commercial viability and sustainability impact; and
(9) Generating research outputs such as—
    a. materials property datasets;
    b. predictive algorithms and analytic models;
    c. physically manufactured prototype materials;
    d. materials digital twins; and
    e. manufacturing sustainability design guidelines and frameworks.

1.5.2.2 Deliverables

OA2 Phase 1 deliverables must include, at a minimum, one or more submissions of:
(1) A refined, stakeholder-informed **Physical Infrastructure Plan**, as needed, including proof of equipment purchases or access agreements.
(2) A refined **Faculty Development Plan** providing details of planned faculty development and demonstrating commitment to building a critical mass of faculty to expand and maintain research capacity.
(3) A **Phase-specific Research Plan** with information on staffing, governance, user management, training, maintenance, experiment type and volume, and other items needed to achieve the Co-optimization Targets.
(4) A **Research Progress Report**, detailing research outputs, lessons learned, and successful research transitions, to include information on—
    a. technoeconomic and lifecycle analyses,
    b. materials and process models, and
    c. industry validation of the above materials and process models.

OA2 Phase 2 and Phase 3 deliverables must include, at a minimum, one or more submissions of:
(1) A refined, stakeholder-informed **Physical Infrastructure Plan,** as needed, including proof of equipment purchases and installation or equipment access agreements.
(2) An updated **Phase-specific Research Plan**, relevant to the phase, to include plans for continued research after the period of performance.
(3) An updated **Research Progress Report**, detailing the development of research outputs.
(4) A **Faculty Development Report**.

1.5.3 OA3: Education and Workforce Development

Across its portfolio, CHIPS R&D expects to support EWD projects that foster a diverse and capable domestic workforce with access to good jobs, such as those consistent with the Departments of Commerce and Labor Good Jobs Principles, a shared federal vision of job quality informing billions of generational investments in advanced manufacturing, clean energy, and infrastructure. The combination of expertise, facilities, equipment, and membership required to execute this NOFO should provide exceptional opportunities for tailored EWD activities. In developing an EWD plan, CHIPS R&D encourages applicants to consult the CHIPS R&D

Education and Workforce Development (EWD) Plan Guidebook as well as the Department of Commerce Workforce Development Strategy Principles.

To demonstrate capabilities relevant to OA3, full applications must include an initial **Education and Workforce Development (EWD) Plan**, including an **EWD Infrastructure and Curriculum Plan**. Applicants are encouraged to propose SMART EWD targets, such as the number of students trained or engaged in research and subsequently placed in good jobs in the domestic semiconductor industry.

To advance best practices and hands-on opportunities for training, CHIPS R&D further encourages applications that provide for outreach and engagement with partner institutions key to the delivery of quality employment and training pathways, such as labor organizations, government agencies, and industry organizations. CHIPS R&D is also interested in applications that indicate engagement with programs focused on training for underserved communities, as defined by Executive Order 13985, Advancing Racial Equity and Support for Underserved Communities Through the Federal Government (Jan. 20, 2021) and Executive Order 14091, Further Advancing Racial Equity and Support for Underserved Communities Through the Federal Government (Feb. 16, 2023).

1.5.3.1 Activities

CHIPS R&D expects activities under OA3 to include developing or expanding one or more of the following:

(1) Paid research assistantships, internships, and fellowships focused on AI/AE activities (at all levels of higher education, including but not limited to undergraduate, masters, doctoral, and post-doctoral); paid research experiences for undergraduates; other university-based research experiences; and if relevant, pre-apprenticeships, registered apprenticeships, and partnerships with employers, labor organizations, community-based organizations, and workforce development boards;
(2) Strategic partnerships with potential employers to ensure alignment of EWD activities with current or future U.S. industry needs, creation of opportunities for students to interact with industry, and creation of pathways for graduating students to enter the domestic semiconductor workforce;
(3) If relevant, curricula and/or degree/certificate programs relevant to AI/AE methods and implementation of effective and evidence-based educational approaches, leading to the development of a skilled and diverse semiconductor workforce through formal and informal education; and
(4) Partnerships with the NSTC Workforce Center of Excellence, to both access and provide access to EWD lessons learned.

CHIPS R&D encourages applicants, in providing an EWD Plan, to describe any efforts to attract and retain a diverse student and trainee population and demonstrate that the EWD efforts that involve employer partners are worker centered, industry-aligned, and promote high-quality jobs.

1.5.3.2 Deliverables

OA3 Phase 1 deliverables must include, at a minimum, one or more submissions of:

(1) A refined, stakeholder-informed **Education and Workforce Development (EWD) Plan**.
(2) An **EWD Progress Report**, detailing progress on Theme 6 Programmatic Targets such as—
    a. the number of students provided significant research experiences in semiconductor-relevant AI/AE; and
    b. the number of graduating students that enter the domestic semiconductor workforce.

OA3 Phase 2 and 3 deliverables must include at a minimum, one or more submissions of:

(1) Updated versions of the **Education and Workforce Development (EWD) Plan**, if applicable; and
(2) An **EWD Progress Report**, detailing progress on Theme 6 Programmatic Targets such as—
    a. progress on Theme 6 Programmatic Targets;
    b. if relevant, new or updated AI/AE-relevant curriculum; and
    c. EWD-relevant lessons learned.

1.6 GENERAL ROLES OF THE AWARD RECIPIENT AND NIST

1.6.1 Substantial Involvement of CHIPS R&D

CHIPS R&D intends to have ongoing and substantial programmatic involvement with the award recipient throughout the award period of performance, aimed at supporting the recipient's activities and working jointly with the recipient in a partnership role. Primary responsibility for the operation and management of the project will reside with the award recipient; however, responsibility for specific tasks and activities may be shared between the recipient and CHIPS R&D, or between the recipient and other NIST organizations, as described below.

1.6.2 Responsibilities of Recipient

CHIPS R&D will require the award recipient to:

(1) Assume primary responsibility for coordination, day-to-day management, and oversight of project activities, financial transactions, reporting obligations, and convening and administration of the project;
(2) Be a collaborative partner with the CHIPS Manufacturing USA Institute, once established, and where appropriate, with relevant components of the NSTC;
(3) If applicable, coordinate with NIST in the development of collaborations with other Federal agencies, including NIST laboratory programs; and
(4) Encourage work environments to implement safety policies, such as NIST's policy for Occupational Safety and Health and any additional NIST guidance on AI safety.

1.6.3 Involvement of NIST and CHIPS R&D

NIST / CHIPS R&D may provide, as appropriate:

(1) Programmatic and financial oversight of the award;
(2) Input relevant to the design and development of activities, including EWD activities;
(3) Subject matter experts to support collaborative research conducted;
(4) Coordination and engagement with other Federal agencies;
(5) Guidance and support related to approvals for membership of foreign-owned organizations;
(6) Research security and other relevant support, as described in Section 1.6 and Section 2.5; and
(7) Advice relevant to applying the voluntary NIST AI Risk Management Framework.

In any award agreement issued under this NOFO, NIST and potentially other Federal agencies may have access to research materials and data, and other outcomes of any funded projects, in accordance with the member agreements, as applicable.

1.6.4 Joint Activities Between Recipient and NIST and CHIPS R&D

For any technical activities that align with NIST's measurement science priorities, NIST may work collaboratively with the recipient, including by organizing workshops or other conferences or partnering with project teams.

1.6.5 Coordination with other Federal R&D Programs

Realizing the full potential of the CHIPS and Science Act requires alignment across programs towards a common strategy and vision. CHIPS R&D may therefore request that the award recipient, as a critical element of the broader CHIPS R&D mission, coordinate closely with other CHIPS R&D programs (NSTC, NAPMP, and CHIPS Metrology) and adhere to the following principles:

(1) CHIPS R&D programs and funding aim to address problems that are of the greatest relevance to the semiconductor industry and align research investments with knowledge gaps, opportunities, and customer demand;
(2) CHIPS R&D programs and funding must prioritize pathways from research to commercialization to ensure long-term economic competitiveness of the U.S. semiconductor industry;
(3) CHIPS R&D programs and funding will avoid unnecessary duplication and competition with each other and with other Federal programs;
(4) CHIPS R&D programs and funding should enable coordination rather than competition among the programs to the greatest extent possible, to leverage activities for maximum impact and long- term sustainability; and
(5) CHIPS R&D programs and funding must contribute to a skilled, diverse semiconductor workforce.

Consistent with the Transition and Impact Strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that commit to collaborate with and support other Federally-funded semiconductor-related R&D initiatives. These initiatives may include, but are not limited to, the U.S. Department of Defense (DoD) National Network for Microelectronics Research and Development, also known as the Microelectronics Commons; Defense Advanced Research Projects Agency (DARPA) Electronics Resurgence Initiative (ERI) and Next Generation Microelectronics Manufacturing (NGMM); National Science Foundation (NSF) Designing Materials to Revolutionize and Engineer our Future (DMREF); semiconductor education activities at NSF and other agencies; as well as other efforts established by the CHIPS and Science Act of 2022 (P.L. 117-167). Further details will become available as these organizations develop their operational plans and membership programs.

1.7 BROADER IMPACTS

CHIPS R&D is committed to building strong communities that share in the prosperity of the semiconductor industry, as well as ensuring that taxpayer investments maximize benefits for the U.S. economy. CHIPS R&D also strongly supports inclusion, diversity, equity, and access, and firmly believes that the semiconductor industry cannot succeed unless all Americans have an opportunity to participate, including individuals from underserved communities. In its evaluation and selection processes, CHIPS R&D will consider how projects will create broader impacts across multiple dimensions described below.

1.7.1 Commitments to Future Investment

Ensuring U.S. leadership in semiconductor technology and the security and resilience of the domestic semiconductor supply chain will require sustained capital, R&D, and workforce investments. In addition to any awards made under this NOFO, significant investment will be required to enable the seamless integration of sustainable materials and processes into the U.S. semiconductor manufacturing industry. CHIPS R&D therefore encourages applications likely to induce non-Federal investment, beyond what would have occurred absent a CHIPS R&D award, into integrating these innovations into domestic manufacturing facilities and equipment. Where feasible, applicants are encouraged to include letters of commitment from potential private sector partners indicating interest in the funded innovation and the potential for industry to rapidly move funded innovations, if successfully demonstrated, to higher TRL levels.

1.7.2 Creating Inclusive Opportunities

The CHIPS for America program strives for the inclusion of a broad array of partners, such as educational institutions, small businesses, minority-owned businesses, veteran-owned businesses, and women-owned businesses.[g] CHIPS R&D will favorably consider applications that, for instance:

(1) Outline robust outreach plans and demonstrate the inclusion of a broad array of partners in the funded activities proposed under this NOFO, such as the businesses described

[g] See Executive Order 14080, 87 Fed. Reg. 52847 (Aug. 25, 2022).

above, as well as educational institutions (e.g., public, private, Historically Black Colleges and Universities (HBCUs), Minority Serving Institutions (MSIs), Tribal Colleges and Universities (TCUs);

(2) Include meaningful leadership opportunities for early career researchers, including individuals from underserved communities and emerging research institutions; and

(3) Provide specific plans for training programs that expand opportunities for participation, including for underserved communities, such as building recruitment partnerships with community-based organizations that have a track record of serving underserved communities, investing in pre-apprenticeship programs, investing in supportive services, and promoting a safe and respectful workforce culture that prevents harassment and discrimination.

1.7.3 Environmental Responsibility

Applicants are encouraged to incorporate strategies for pollution prevention, energy efficiency, water efficiency, and renewable energy use in their proposed approach. The Department expects applicants to design their projects so that they avoid, minimize, or mitigate the potential for significant effects on the human environment.

1.7.4 Community Impact and Support

Consistent with the transition and impact strategy evaluation criterion (see Section 5.3.4), CHIPS R&D will favorably consider applications that demonstrate the impact of the project on creating long-lasting new participants in the semiconductor innovation ecosystem. Other positive factors could include the ability of the research outputs, if successful and adopted, to support the creation of good jobs, including for individuals from underserved communities. For the purposes of this NOFO, applicants seeking to demonstrate community impact and support, including impacts on a new or existing regional semiconductor industry cluster, can do so in a variety of ways, including through:

(1) Letters of commitment or interest submitted by community-based organizations, civil society or labor organizations, and local officials;

(2) Letters of commitment or interest from industry partners, noting the benefit of sustainable semiconductor materials and processes to a domestic semiconductor industry cluster, which may be in a region other than the applicant; and

(3) Alignment with regional, state, or local economic development strategies, assets, resources, or capacities, such as relevant Comprehensive Economic Development Strategies, Workforce Innovation and Opportunity Act (WIOA) state and local workforce plans, regional or cluster-based growth efforts, or other complementary Federal investments under programs such as the DOC Build Back Better Regional Challenge (BBBRC). DOC Regional Technology and Innovation Hub (Tech Hubs) program, or NSF Regional Innovation Engines program, including through strong, concrete commitments to such programs' consortia and participation in consortium/coalition governance.

1.8 GOVERNMENT-FURNISHED PROPERTY (GFP) AND GOVERNMENT FURNISHED INFORMATION (GFI)

Under this NOFO, no GFP or GFI is identified to be provided at this time. Availability will be determined for each award on a case-by-case-basis.

2 FEDERAL AWARD INFORMATION

2.1 FUNDING AVAILABILITY

The funding amounts referenced in this NOFO are subject to the availability of funds and the Department's priorities at the time of award. The Department is not responsible for any application preparation costs. Publication of this funding opportunity announcement does not obligate the Department to make any specific award or to obligate any available funds. Subject to the availability of funds and based on the quality of applications received, CHIPS R&D anticipates making up to three awards ranging from approximately $20 to $40 million per award, with a period of performance of up to five years. Total Federal funding available under this NOFO for all awards is expected to not exceed approximately $100 million. CHIPS R&D reserves the right not to make any award under this NOFO, based on the quality of applications received, program priorities, and the availability of funds.

2.1.1 Funding Instrument and Payments

Awards in this program will be made as other transaction agreements (OTAs), as authorized by 15 U.S.C. § 4659(a)(1), which provide the Department the flexibility to create award agreements reflecting the unique, innovative nature of this program.

2.1.2 Multi-Year Funding Policy

If an application under this NOFO for a multi-year award is approved, funding will be provided only for the first phase of the project; additional phases will be funded incrementally. Funding for subsequent phases will be contingent upon the recipient's satisfactory performance; the award's continued relevance to the CHIPS R&D mission, goals, and priorities; and subject to the availability of funds.

CHIPS R&D reserves the right to suspend or terminate an award if phase-specific targets, milestones, and deliverables are not met, for non-performance or under-performance under the award agreement, or non-compliance with award terms and conditions, as applicable.

2.2 ELIGIBLE USES OF FUNDS

Eligible uses of Federal funds under this NOFO include operational activities to execute the project; basic and applied research related to AI/AE for sustainable semiconductor materials and processes; the procurement, upgrade, or maintenance of necessary research equipment at universities; accessing such equipment outside of academia or outside of the project team;

industry-relevant demonstration projects and technology transition activities; and education and workforce development. Where consistent with the objectives of this NOFO, applicants may also propose to expend limited funds to protect innovations developed under this NOFO, including to cover fees for patent protection or to enhance research security. In addition, applicants may propose, subject to NIST's approval, to expend funds for the applicant and a limited number of Project Team members to join the CHIPS Manufacturing USA Institute and NSTC, for the purpose of supporting this program.

2.2.1 Construction

Construction activities are generally not an allowable cost with Federal funds under this NOFO. However, costs related to internal modifications of existing buildings that may be necessary to carry out the proposed research tasks may be allowed, as determined by NIST in its sole discretion, and, where applicable, subject to the prevailing wage requirements under 42 U.S.C. § 3212.

Certain activities may be subject to various Federal, state, and local environmental and permitting requirements, such as under the National Environmental Policy Act (NEPA), National Historic Preservation Act (NHPA), Endangered Species Act, Clean Water Act, Clean Air Act, Resource Conservation and Recovery Act, and related Executive Orders. Applicants must assist the Department with compliance with the above referenced requirements and, where applicable, are responsible for obtaining all necessary permits for the project and complying with any applicable Federal, state, and local laws and regulations.

CHIPS R&D will review invited full applications to determine whether they provide sufficient information to support NEPA and NHPA reviews, and may, in its sole discretion, request the applicant to provide additional information. The Department may request that an applicant prepare draft environmental analyses, which it will review to determine the potential environmental impacts and consultation needs of proposed activities under consideration for use of Federal funds under this NOFO. CHIPS R&D may also request further supplementary written information or may ask questions during pre-selection interviews and/or site visits. CHIPS R&D will not issue any award under this NOFO until any required environmental reviews under NEPA for that award has been completed.

2.2.2 Indirect (F&A) Costs

CHIPS R&D will reimburse applicants for proposed indirect costs, commonly referred to as Facilities & Administrative (F&A) Costs, in accordance with this subsection. Applicants with a current negotiated indirect cost rate may use up to their Federally approved indirect rate to budget for indirect costs. Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of fifteen (15) percent of modified total direct costs (MTDC). Applicants proposing indirect costs must follow the application requirements set forth in Sections 4.6.1.8 and 4.6.1.9 of this NOFO.

2.3 PUBLIC ACCESS TO CHIPS R&D RESEARCH

NIST is committed to the principle that the results of Federally funded research are a valuable national resource and a strategic asset. To the extent feasible and consistent with law, agency mission, resource constraints, and U.S. national, homeland, and economic security, NIST will promote the deposit of scientific data arising from unclassified research and programs, funded wholly or in part by NIST, except for Standard Reference Data, free of charge in publicly accessible databases. Subject to the same conditions and constraints listed above, NIST also intends to make freely available to the public, in publicly accessible repositories, all peer-reviewed scholarly publications arising from unclassified research and programs funded wholly or in part by CHIPS R&D.

Any applications for activities that will generate research data (see 2 C.F.R. § 200.315(e)(3)) using Federal funds awarded under this NOFO are required to adhere to a Data Management Plan (DMP) or explain why data sharing and/or preservation are not within the scope of the project (see Section 4.6.1.12).

2.4 FUNDAMENTAL RESEARCH

National Security Decision Directive (NSDD) 189 defines "fundamental research" as follows:

> *'Fundamental research' means basic and applied research in science and engineering, the results of which ordinarily are published and shared broadly within the scientific community, as distinguished from proprietary research and from industrial development, design, production, and product utilization, the results of which ordinarily are restricted for proprietary or national security reasons.*

Funded activities under this NOFO may include efforts categorized as fundamental research. In submitting an application, the applicant acknowledges that research activities considered to be fundamental research may include or produce IP with relevance to U.S. national or economic security and that requires protection against foreign interference and exploitation. As such, the applicant and any subrecipients agree to comply with the research security requirements described in Section 2.5 of this NOFO.

2.4.1 Fundamental Research Declaration

NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental research. However, applicants must indicate in the Project Narrative (see Section 4.6.1.6) whether, in the applicant's understanding, the proposed work includes fundamental research conducted either by the applicant or by any subrecipient members of the project team.

2.4.2 On-Campus Research

Wherever feasible, NIST/CHIPS will consider basic or applied research conducted on campus at a university as fundamental research.

2.4.3 Pre-Publication Reviews

Awards made under this NOFO that include fundamental research will include appropriate language reaffirming the ability of the applicant and members of the project team to publish and share broadly the results of such fundamental research.

Awards made under this NOFO that include research not deemed fundamental will prescribe publication requirements and other restrictions, as appropriate, for such research. This may include requirements for the applicant to submit publications describing work carried out under this program for an efficient pre-publication review by NIST/CHIPS R&D. The pre-publication review may result in a request for revisions to address national security concerns. The pre-submission review may also include an assessment of and advice to the award recipient regarding whether information disclosed in the publication could negatively impact the patent interests of either the award recipient or the Government.

2.5 RESEARCH SECURITY

It is NIST policy to create a culture of personal and organizational responsibility where the practice and management of research and its products are free from undue influence and interference not essential to the practice of science, such as personal or social allegiances, beliefs, or interests. NIST adheres to the principle that U.S. research leadership benefits from mutually beneficial international collaborations, including welcoming international scientists, and that U.S. national and economic security depends on effective risk management practices for all research organizations to protect against foreign interference and exploitation. Founded on NIST's core values of perseverance, integrity, inclusivity, and excellence, the NIST Research Security Team promotes mutually beneficial international engagement using a risk-based methodology to safeguard NIST research programs and intellectual property.

2.5.1 Research Security Definitions

Unless otherwise noted, the definitions for terms used in this section are found in the Appendix to Guidance for Implementing National Security Memorandum 33 (NSPM-33) on National Security Strategy for United States Government-Supported Research and Development issued by the National Science and Technology Council in January 2022.

2.5.2 Authorities

In recent years, both Congress and the Executive Branch have focused on protecting R&D conducted or funded by Federal agencies from undue foreign influence. On January 14, 2021, National Security Presidential Memorandum-33 (NSPM-33) was issued to "strengthen protections of United States Government-supported R&D against foreign government interference and exploitation." NSPM-33 requires U.S. agencies that fund R&D to require the

disclosure of information related to potential conflicts of interest and commitment from participants in the Federal R&D enterprise.

Under Section 223 of Division A, Title II of the William M. (Mac) Thornberry National Defense Authorization Act (NDAA) for Fiscal Year 2021 (FY21), (Pub. L. No 116–283, codified at 42 U.S.C. § 6605), "covered individuals" (see Section 2.5.4) must disclose the amount, type and source of all current and pending research support, which includes both monetary and non-monetary support, and certify that the disclosure is current, accurate, and complete as part of the application for an R&D award. In addition, covered individuals must agree to update disclosures, as required, before and during the term of the award.

Subtitle D of Title VI of the Research and Development, Competition, and Innovation Act, enacted along with the CHIPS and Science Act of 2022, codified at 42 U.S.C. § 19231 – 19237, also contained research security requirements.

On February 14, 2024, the Office of Science and Technology Policy (OSTP) defined the term "foreign talent recruitment program" in issuing Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment Programs required under 42 U.S.C. § 19231(b). Also, on July 9, 2024, the Office of Science and Technology Policy (OSTP) released Guidelines for Research Security Programs at Covered Institutions.

The research security provisions in this NOFO are consistent with all authorities cited in this section, as applicable.

2.5.3 Requirement for a Research Security Plan or Program

Under this NOFO, applicants must submit a written plan (see Section 4.6.1.6)—

(1) identifying a member of applicant's leadership team to serve as the point of contact responsible for coordinating with NIST on research security issues;
(2) describing internal processes or procedures to address foreign talent recruitment programs (as referenced in Section 2.5), conflicts of commitment, conflicts of interest, research security training, and research integrity;
(3) describing measures taken to ensure that appropriate practices for cybersecurity, such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs), are incorporated in the project; and
(4) listing any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51).

Pursuant to the authorities described above, for any applicant that meets the definition of a "covered institution"[h], the Research Security Plan must further describe its intent to establish and

[h] The July 9, 2024, OSTP Guidance defines "covered institution" as an institution (A) of higher education, a federally funded research and development center (FFRDC), or a nonprofit research institution; and (B) that receives in excess of $50 million per year, in fiscal year 2022 constant dollars, under (1) the three-year average of

operate a Research Security Program (see Section 2.5). Applicants can refer to the CHIPS R&D Research Security and Technology Protection web page for additional information.

In August 2023, NIST published the Safeguarding International Science: Research Security Framework (NIST IR 8484), which provides (1) guidance on establishing a successful Research Security Program; (2) background information related to research security generally; and (3) methodologies and requirements for an integrated, mission-focused, risk-balanced approach for safeguarding international science and technology from undue foreign interference while protecting the openness and integrity of the U.S. research ecosystem. In addition, CHIPS R&D published a companion document, the CHIPS Technology Protection Guidebook, as a resource for implementing applicant and performer research security requirements.

Upon review of the applicant's Research Security Plan, NIST may provide the applicant with feedback and an opportunity to refine the Plan, as described in Section 2.5.8.

By submitting an application under this NOFO, an applicant—regardless of its status as a "covered institution"—acknowledges that, if preliminarily selected for an award, it has the capacity to demonstrate, prior to receipt of the award, that CRDO-funded research and associated data products will be protected. The applicant further acknowledges that NIST/CHIPS may deem implementation of certain elements of a Research Security Plan as a condition of the award.

2.5.4 Covered Individuals

For the purposes of this NOFO and as defined under 42 U.S.C. § 6605(d)(1), the term "covered individual" is defined as "an individual who (1) contributes in a substantive, meaningful way to the scientific development or execution of a research and development project proposed to be carried out with a research and development award from a Federal research agency; and (2) is designated as a covered individual by the Federal research agency concerned."

In developing the Project Narrative required under Section 4.6.1.6, the applicant must determine and identify which individuals are covered individuals and provide a brief description (title or one-sentence summary) of the role to be served by each covered individual. Applicants must also complete the Current and Pending Support Forms required under Section 4.6.1.13.

Covered individuals must include any identified principal investigators, co-investigators, and associate investigators and any individual listed under Section 4.6.1 by the applicant as "key personnel" or as a "Senior/Key Person" or for whom a resume or CV is included. Personnel who participate only through isolated tasks that are incidental to the research (for example, setting up equipment or performing administrative functions), and those individuals who support research

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federal R&D obligations provided to participants in the U.S. R&D enterprise as reported in the most recent version of the Survey of Federal Science and Engineering Support to Universities, Colleges, and Nonprofit Institutions; or (2) the three-year average of federal R&D obligations to FFRDCs as provided in the most recent versions of the Survey of Federal Funds for Research and Development.

by executing discrete tasks as directed are not covered individuals. Consistent with guidance for implementing NSPM-33, disclosures from broader classes of individuals (e.g., certain graduate students and undergraduate students) will generally be unnecessary, except when the activities of such an individual in a specific proposal rise to the level of meeting the definition of a "covered individual" under 42 U.S.C. § 6605(d)(1).

2.5.5 Foreign Entities of Concern

Pursuant to 15 U.S.C. § 4657, Federal funds awarded under this NOFO shall not be provided to any "foreign entity of concern," as that term is defined in 15 U.S.C. § 4651(8) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600[i] (Sept. 25, 2023), codified at 15 C.F.R. § 231.104. Foreign entities of concern are also ineligible to participate in this NOFO as unfunded collaborators.

To ensure compliance with this requirement, applicants to this NOFO must submit a Written Summary of Certain Research Partnerships or Technology Transfer Commitments (see Section 4.6.1). This document should describe any research partnerships or technology transfer commitments in areas relevant to the activities within this NOFO or any other areas related to the mission and goals of CHIPS R&D (see Section 1.1.1) between the applicant entity and (a) any entities located in a foreign country of concern or (b) with any entities that are foreign entities of concern.[j]

2.5.6 Research Security Review and Risk Determination

The NIST Research Security Team will conduct a preliminary research security review and a risk determination of concept papers initially identified for invitation to full application and may conduct a subsequent review and risk determination of submitted full applications. During the review, NIST will use NIST IR 8484 as the basis for reviewing and assessing research security risks. In conducting this review, NIST will review available information, (e.g., the Current and Pending Support Form and Resume or CV) to assess whether the applicant or any covered individuals, including foreign nationals who are not lawful permanent residents or protected persons as defined in 8 U.S.C. § 1324b(a)(3), are subject to any undue foreign influence or interference through conflicts of interest or conflicts of commitment. Undue foreign influence or interference may include, but is not limited to, associations or affiliations with foreign strategic competitors or governments of countries that have a history of intellectual property theft, research misconduct, or targeting U.S. technology for unauthorized transfer. Affiliations include any past or present organization (foreign and domestic) with whom the applicant has a formal relationship or obligation (e.g., universities, scholarships, professional societies, foreign talent recruitment programs).[k] NIST will examine associations or affiliations during the ten-year period immediately preceding the application submission.

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[i] See https://www.federalregister.gov/documents/2023/09/25/2023-20471/preventing-the-improper-use-of-chips-act-funding

[j] Covered Individuals should separately detail potential research activities or technology transfer commitments within their Current and Pending Support forms

[k] See OSTP Guidelines for Federal Research Agencies Regarding Foreign Talent Recruitment Programs

At the conclusion of the research security review for the application, NIST will issue a determination of low, medium, or high risk. NIST will base its risk determination of the proposal on the totality of information, which may include but is not limited to:

(1) The ownership structure, subsidiaries, and obligations of the applicant, the project team (including subrecipients or unfunded collaborators);
(2) Conflicts of interest and conflicts of commitment of covered individuals;
(3) Participation of covered individuals in a foreign talent recruitment program; and
(4) Any military-civil applications of the funded research, as applicable.

Regardless of the risk determination and at its sole discretion, NIST may request clarifying information, or work with the applicant to mitigate the assessed risks (see Section 2.5.8). NIST may contact the applicant at any time after receipt of its concept paper or full application, to seek relevant clarifications or risk mitigation, including during the merit review or evaluation process.

2.5.7 Non-Discrimination Policy

Consistent with Section 10637 of the CHIPS and Science Act of 2022 and Executive Orders 13985 and 14031, NIST activities that implement NSPM-33 and 42 U.S.C. § 6605 are carried out in a manner that does not inadvertently target, stigmatize, or discriminate against individuals on the basis of race, color, ethnicity, religion, sex (including pregnancy, sexual orientation, or gender identity), national origin, age (40 or older), disability, and genetic information (including family medical history), consistent with Title VI of the Civil Rights Act of 1964 (42 U.S.C. § 2000d et seq.).

2.5.8 Potential for Mitigation

NIST may, at its sole discretion, provide the applicant an opportunity to mitigate any assessed risks prior to CHIPS R&D making a final determination to select either the concept paper or full application. NIST/CHIPS R&D reserves the right to request specific mitigation actions, including but not limited to requiring additional training for project participants or segmentation of certain tasks of the proposed work, and any follow-up information needed to assess risk or mitigation strategies. CHIPS R&D may determine not to make an award, despite any proposed mitigation terms in connection with an application.

2.5.9 Requirement for Recipients to Update Research Security-Related Information

Pursuant to 42 U.S.C. § 6605(a)(1)(C), applicants have an ongoing duty to inform the NIST Agreements Officer of any changes made to the list of covered individuals or to the foreign affiliations and research financial and in-kind support of such individuals or of the applicant and any subrecipients. Prior to NIST making an award under this NOFO, applicants must inform the NIST Agreements Officer of any such changes immediately. During the period of performance, award recipients must update the NIST Agreements Officer within five (5) business days of any such changes being made or of becoming aware of any such changes.

Applicants and subrecipients are expected to exercise due diligence to ensure that covered individuals involved in the subject award are not subject to foreign interference or exploitation.

2.6 INTELLECTUAL PROPERTY (IP) AND DOMESTIC PRODUCTION

2.6.1 Intellectual Property

As set forth in 15 U.S.C. § 4656(g), the Department of Commerce must "develop policies to require domestic production, to the extent possible, for any intellectual property" resulting from R&D conducted using Federal funds awarded under this NOFO. Further, 15 U.S.C. § 4656(g) requires CHIPS R&D to develop domestic control requirements to protect any such IP (which may include software) from foreign adversaries. For the purposes of 15 U.S.C. § 4656(g), "intellectual property" means any invention that is or may be patentable under U.S. law; and "foreign adversaries" include any "foreign entity of concern" and "foreign country of concern," as those terms are defined in 15 U.S.C. § 4651(7)-(8) and 15 C.F.R. §§ 231.102, 231.104, as well as any entity whose actions, policies, or personnel decisions are controlled by a "foreign entity of concern" or "foreign country of concern."

2.6.2 Domestic Production

For the purposes of 15 U.S.C. § 4656(g) and the commercial viability and domestic production plan later described, "production" includes the manufacture, integration, assembly, testing, and packaging of semiconductors, materials used to manufacture semiconductors, or semiconductor manufacturing equipment developed or improved as a result of CHIPS-funded intellectual property. Applicants under this NOFO should describe their intent to maximize domestic production in the CVDP and, as appropriate, Intellectual Property Rights Management Plan. CHIPS R&D does not require the covered production to occur exclusively within the United States. However, applicants that are unable to conduct certain production activities in the United States should explain within their CVDP, to the extent practicable at the current level of technology development, why such production may not be possible, considering the following factors:

(1) The availability or lack of availability of domestic production capabilities, which may consider:
    a. Planned or previous efforts made to locate, develop, or contract for the production of the CHIPS R&D-funded technology, or relevant similar technologies, in the United States;
    b. Access to resources and other material inputs required for production; and
    c. The expected additional product development time or cost required to make U.S. production of the CHIPS R&D-funded technology commercially feasible;
(2) The relative costs of domestic versus foreign production of the CHIPS R&D-funded technology, at relevant production volumes;
(3) Commercial adoption risks and benefits, such as:
    a. Risks to the market acceptance and to the value proposition for the CHIPS-funded technology, resulting from U.S. production; and

b. Expected commercial, economic, or national security benefits to the United States resulting from distributed production among U.S. and overseas sites; and

(4) Any other factors that are important to the success of the CHIPS R&D-funded technology.

2.6.3 Domestic Control

To meet the requirements of 15 U.S.C. § 4656(g), CHIPS R&D will include special award terms and conditions related to intellectual property and domestic control. The relevant terms and conditions will include, at a minimum, the following:

(1) At least one domestic entity must own or co-own any intellectual property resulting from R&D (e.g., applicant or sub-recipient) conducted under this NOFO ("resulting intellectual property") and must have full rights to enforce the applicable intellectual property rights, at least for a period of years to be determined prior to the final award;

(2) At the conclusion of the period of years, ownership of the resulting intellectual property may generally be sold, transferred, or assigned to a foreign entity that is not a foreign adversary;

(3) In the event a domestic entity sells, transfers, or assigns ownership of the resulting intellectual property, the entity must promptly disclose such transaction to NIST prior to such transaction;

(4) Any owner or co-owner of the resulting intellectual property (including successors in interest) may not sell, transfer, or assign ownership of such intellectual property to a foreign adversary;

(5) Any owner of the resulting intellectual property may not license such intellectual property to a foreign adversary, subject to the following specific exceptions;

a. This restriction is not applicable to the following specific exceptions, provided that an owner or co-owner of any patent or patent application resulting from R&D conducted under this NOFO satisfies the notification requirement specified in 5.a.iii below:

i. This restriction is not applicable to any patent(s) or published patent application(s) (i) declared and/or determined to be essential to a technical standard and (ii) under an obligation that the owner of the patent or published patent application license such rights pursuant to the terms of a standards development organization's Intellectual Property Rights policy.

ii. This restriction is not applicable to any license(s) of patent(s) or published patent application(s), including cross-licenses, resulting from settling an actual case or controversy, including patent infringement or validity disputes, whether part of a formal proceeding or not.

iii. In the event an owner or co-owner of the patent(s) resulting from R&D conducted under this NOFO determines that any of the specific exceptions above applies and plans to license such patent(s) to a foreign adversary

pursuant to the exception(s), the owner or co-owner must promptly disclose such action for NIST review.

b. This restriction is not applicable to the sale of a product by a funding recipient (or any other lawful owner, assignee, transferee or licensee of the IP) and any accompanying implied or explicit intellectual property license relating to the use of the product that is sold.

2.6.4 Commercial Viability and Domestic Production Plan (CVDP)

In keeping with the provisions of Executive Order 14104 and the CHIPS Act domestic production requirements (15 U.S.C. § 4656(g)), CHIPS R&D requires applicants to develop and provide a Commercial Viability and Domestic Production (CVDP) plan describing activities to be funded as part of their application. To assist in the development of CVDP plans, CHIPS R&D has published a CHIPS R&D Commercial Viability and Domestic Production Plan Guidebook.

Applicants should be aware that the CVDP represents an initial assessment of the commercial viability and domestic production opportunities of potential funded research outputs, with updates occurring across the award period. Given this NOFO's focus on industry-informed, university-based collaborations, CHIPS R&D anticipates that Phase 1 Theme 7 targets may largely focus on strengthening industry partnerships, conducting technoeconomic analyses, and informing the CVDP. CHIPS R&D expects that awardees will refine more definitive applicant-proposed metrics for technology transfer during Phase 1, for tracking during Phases 2 and 3.

Depending on the size and scope of the project award, a strong CVDP plan should include, to the extent possible, a realistic business model for the funded innovations (which may include software), include a technology transition plan, and describe pathways to benefitting national and economic security, such as through the domestic availability of the technology and successful adoption by commercial or defense partners. Applicants must propose measurable CVDP targets that demonstrate the viability of the proposed business model and of domestic production. Where relevant, CVDP milestones should complement technical milestones. Applicants can strengthen these targets and milestones across the award period, in response to technoeconomic analyses and technical achievements.

Strong CVDP plans should present evidence of existing or potential demand for the funded innovations; identify existing or potential customers, or categories of customers, at volumes necessary for commercial viability; provide an initial assessment of marketability in terms of cost and value proposition that can be updated as the project advances; describe existing or potential competitors and competing technologies; and demonstrate the potential to attract private capital, such as venture capital. Given this NOFO's focus on industry-informed, university-based collaborations, certain CVDP elements (e.g., detailed marketability assessments) may be deferred until Phase 1 of the award. In lieu of these elements, CHIPS R&D strongly recommends that the applicant provide letters of interests or letters of commitment demonstrating private sector support for the proposed research outputs.

CHIPS R&D strongly encourages applicants to identify approaches to maximizing market advantages of the funded innovation, such as by reducing manufacturing costs and improving yields (e.g., optimizing process times and achieving economies of scale through increasing volume). These approaches align with the Theme 1 metrics.

CHIPS R&D further encourages applicants to outline mechanisms (which may include licensing strategies) to encourage domestic adoption, deployment, and integration of the funded innovation into domestic manufacturing processes and supply chains.

Finally, CHIPS R&D recognizes the importance of preventing the illicit exfiltration of funded innovations, including software, in order to protect competitive advantage. Successful CVDP plans may therefore also consider security and compliance measures to mitigate risks associated with the unauthorized access to the funded innovation, which may include encryption, access controls, authentication mechanisms, and adherence to relevant cybersecurity standards and regulations.

To assist in the development of CVDP plans, CHIPS R&D has published a CHIPS R&D Commercial Viability and Domestic Production Plan Guidebook.

Applicants must refine and update the CVDP plan during the period of performance, at a minimum before the end of each award phase. Applicants must also submit an IPRM, as outlined in Section 4.6.1.6, and will be required to provide regular updates to the IPRM to report any new intellectual property or any new or modified intellectual property governance structures.

For the purposes of this NOFO, CHIPS R&D strongly suggests that applicants work with industry partners to determine the commercial viability of the proposed research outputs, where relevant. However, there may be cases where the research outputs may not yield commercial sales at volume or may not be subject to production (e.g., models).

3 ELIGIBILITY INFORMATION

3.1 ELIGIBLE APPLICANTS AND SUBRECIPIENTS

Under this NOFO, eligible applicants are domestic accredited institutions of higher education and domestic non-profit or for-profit organizations that manage consortia of accredited institutions of higher educations. A domestic entity is one that is incorporated within the United States (including a U.S. territory) with its principal place of business in the United States (including a U.S. territory). Eligible applicants may submit only one concept paper and, if invited, one full application.

Eligible subrecipients include accredited institutions of higher education; for-profit organizations or non-profit organizations; State, local, territorial, and Tribal governments; Federally Funded Research and Development Centers; Federal entities; foreign partners; and other entities that are eligible to participate as applicants under this NOFO. Eligible subrecipients may be included in more than one application.

CHIPS R&D strongly encourages applications from multi-disciplinary, multi-organization project teams that collectively demonstrate the full range of expertise, experience, and development capabilities needed to achieve the objectives of this NOFO. Prospective funded and unfunded partners, such as industry organizations and civil society or labor organizations, for instance, can play a significant role in ensuring that initial and refined Co-optimization Targets and the resulting Phase-specific Research Plans meet industry needs and support both technology commercialization, environmental sustainability and human health and safety. Strong proposals should identify within the Project Team Description the expected roles of each such organization, including on the Research Advisory Board or in similar mechanisms to receive regular stakeholder guidance.

Consistent with the direction under Executive Order 14080 (Implementation of the CHIPS Act of 2022) for agencies to prioritize benefitting a broad range of stakeholders and to establish collaborative networks, CHIPS R&D encourages that proposals include recipients or subrecipients such that awards significantly expand the capabilities of emerging research institutions in partnership with industry, other research universities, and national laboratories.

Prospective applicants and subrecipients are required to have an active registration in the System for Award Management (https://sam.gov/content/home) and are encouraged to begin the process of registering as early as possible.

3.1.1 Federally Funded Research and Development Centers

Federally Funded Research and Development Centers (FFRDCs) may participate in awards as subrecipients or as contractors, to the extent allowed by law, based on the unique and specific needs of the proposed project.

Applicants must identify the FFRDC(s) in the Project Narrative and provide documentation attached to the required letter of commitment (see Section 4.6.1.11) establishing that FFRDC subrecipients or contractors are able to participate in the proposed work, including:

(1) Documentation demonstrating that the proposed work does not compete with the private sector; and
(2) Documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive federal funding opportunities; the FFRDC's compliance with the sponsor agreement; and confirmation from the sponsoring agency that they can receive Federal funds from NIST.

FFRDCs interested in participating in an award made under this NOFO should first contact their sponsoring agency to discuss their eligibility to receive Federal funds under this NOFO.

3.1.2 Federal Entities

Federal entities (e.g., Federal departments and agencies, military services educational institutions, etc.) are eligible to participate in this NOFO as subrecipients or contractors, to the extent allowed by law and subject to applicable direct competition limitations. Federal entities must clearly demonstrate that the work is not otherwise available from the private sector and provide written documentation citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry.

Applicants must identify in the Project Narrative any proposed Federal entity that would participate as a subrecipient or contractor and provide documentation attached to the required letter of commitment (see Section 4.6.1.11) establishing that the Federal entity is able to participate in the proposed work.

3.1.3 Individuals and Unincorporated Sole Proprietors

Individuals and unincorporated sole proprietors are not eligible to receive funding under this NOFO.

3.1.4 Foreign Partners and Foreign Research Activities

Subject to CHIPS R&D review and approval, foreign organizations may participate as members of a project team, as subrecipients or as contractors, provided that they are not a foreign entity of concern. In each case, the applicant leading a project must be a domestic entity. For the purposes of this section, a foreign entity is any entity that is not a domestic entity. A domestic entity includes the following: (1) a State, local, or Tribal government in the United States; or (2) any entity that is (a) organized under the laws of the United States or any jurisdiction within the United States and (b) has a principal place of business in the United States.

3.1.4.1 Foreign Partner Justification

Under this NOFO, CHIPS R&D must provide the applicant with written approval for a foreign partner's participation in a funded project prior to the foreign partner engaging in any project-related work. Such participation may include receipt of CHIPS funding, receipt of CHIPS-funded intellectual property, or research activities occurring outside of the United States. The applicant must provide CHIPS R&D with a written justification demonstrating:

(1) That the foreign partner's involvement is essential to advancing program objectives, such as by offering access to unique facilities, IP, or expertise that is otherwise not readily available in the United States;
(2) The adequacy of any agreements and protocols between the applicant and foreign partner regarding IP protection and data protection;
(3) The partnership does not jeopardize the soundness of the project's proposed pathway to domestic production;

(4) As applicable, the foreign partner will comply with any necessary nondisclosure agreements, security regulations, export control laws, audit requirements, and other governing statutes, regulations, and policies;
(5) The foreign entity is not based in a "foreign country of concern," as that term is defined at 15 U.S.C. § 4651(7) and implemented by the final rule entitled Preventing the Improper Use of CHIPS Act Funding, 88 FR 65600 (Sept. 25, 2023), codified at 15 C.F.R. § 231.104; and
(6) The foreign partner agrees to be subject to a security review by CHIPS R&D, which may include a risk assessment of IP leakage, if appropriate.

3.1.4.2 Location of funded activity

While the work funded under this NOFO is to be conducted within the United States, certain tasks outside the United States may be allowed based on the unique and specific capabilities available at the foreign location, their relevance to the project objectives, and the lack of comparable capabilities in the United States. In its sole discretion, CHIPS R&D's determination regarding the performance of project tasks outside the United States, whether by a domestic entity of a by a foreign partner, will be based on information provided by the applicant and by other Federal agencies.

CHIPS R&D will only approve work outside of the United States only if it is in the best interest of CHIPS R&D and the United States, including the domestic economy generally, U.S. national security, U.S. industry, and U.S. manufacturing competitiveness. In making such a determination, CHIPS R&D will consider whether the proposed non-domestic activity advances the economic or national security interests of the United States and the justification described in Section 3.1.4.1. CHIPS R&D will not approve the disbursement of any funds awarded under this NOFO to an entity in or under the control of a foreign country of concern under any circumstances.

3.2 OPTIONAL CO-INVESTMENT

A key goal of this NOFO is to have a significant impact on the semiconductor industry. To fully achieve that goal, CHIPS R&D encourages applicants to identify, within the Project Narrative, opportunities for co-investment from partners, to support the development and eventual deployment of research outputs.

Examples of co-investment may include those commitments required. Examples of optional co-investment may include:

(1) Provision of expert time during the period of performance, such as to identify industry-relevant materials and processes and Co-optimization Targets or to provide guidance on research directions via the Research Advisory Board;
(2) Provision of facilities and equipment to research institutions during the period of performance, to support the conduct of research;
(3) Provision of access to private-sector facilities, equipment, and training during the period of performance; and

(4) Commitments of future private sector funding to enable the scale-up, commercialization, and transition to domestic production of funded innovations, beyond activities funded under this award or potentially following the period of performance.

3.3 ALLOWABLE COSTS

For the purposes of submitting an application under this NOFO, allowable costs are generally determined in accordance with cost principles similar to those provided under 2 C.F.R. Part 200, Subpart E. For final award costs, NIST may, in its sole discretion, accept costs that would not be allowable under 2 C.F.R. Part 200, Subpart E, provided that the proposed costs are allocable to and necessary for the success of the project and approved in writing by NIST.

4 APPLICATION AND SUBMISSION INFORMATION

4.1 OVERVIEW

The application process consists of a mandatory concept paper and a full application. Full applications will be accepted only from applicants that are invited after completion of the concept paper stage. Eligible applicants may submit only one concept paper and one full application, if invited, under this NOFO. See Section 3 regarding eligibility requirements.

CHIPS R&D may make changes or additions to this NOFO at any time, including, for example, adjustments to submission deadlines or other requirements. All changes will be communicated through Grants.gov. It is recommended that applicants set up a Grants.gov account and subscribe to this funding opportunity announcement in order to be notified of any updates or changes. CHIPS R&D may also close or withdraw this NOFO with at least 60 days' notice and is not obligated to make any Federal award or commitment as a result of publishing this announcement.

All submissions must be unclassified. The Department will not reimburse applicants for any costs associated with participation in this NOFO. Likewise, the cost of preparing concept papers and full applications in response to this NOFO is not an allowable cost (direct or indirect) under any Federal award.

4.2 WHERE TO OBTAIN AN APPLICATION PACKAGE

The application package for concept papers and full proposals is available at Grants.gov under Funding Opportunity Number 2025-NIST-CHIPS-AIAE-Sustainability-01.

4.3 PAGE COUNT GUIDANCE

This NOFO identifies strict limitations on page counts for the concept paper and, where invited, a full application. As part of its initial administrative review, CHIPS R&D will redact any pages received in excess of the stated page limits prior to beginning the merit review. The applicant should refer to Table 3 and Table 4 to determine which documents and forms are included and excluded in page count limits for concept papers and full applications, respectively.

4.4 SUBMISSION FORMAT

Applicants should follow the guidance and information provided at Grants.gov and in Section 4.5 and Section 4.6 of this NOFO for concept paper and full application submissions, respectively, which includes requirements for uploading specific forms and plans. A concept paper or full application received after the specified date and time will NOT be considered for an award.

Applicants should carefully follow specific Grants.gov instructions to ensure that all attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicating that an application has been received does not provide information about whether attachments have been received. For information or questions regarding applying electronically for the 2025-NIST-CHIPS-AIAE-Sustainability-01 NOFO, contact the Grants.gov Help Desk at 800-518-4726.

Document formatting requirements are specified to ensure the readability of the document by reviewers. Neither the concept paper nor full application should contain any hyperlink references used solely to circumvent any page restrictions. All required information must be contained within the specified page limits provided in Table 3 and Table 4 below for the concept papers and full applications, respectively.

4.4.1 Amendments

Any amendments made to this NOFO will be announced through Grants.gov. Applicants may sign up on Grants.gov to receive notification of any amendments by e-mail.

4.4.2 Proprietary and Sensitive Business Information

Applicants must clearly identify proprietary information in their concept papers and full applications. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as “Proprietary” or “Sensitive Business Information” and provide an indication as to what specific information is proprietary or sensitive.

Applicants must not submit any classified information.

4.5 CONCEPT PAPER INSTRUCTIONS

The required content and form of concept papers submitted pursuant to this NOFO are set forth below.

4.5.1 Required Forms and Documents

Standard Form (SF)-424 (R&R), Application for Federal Assistance. Instructions for completing the SF-424 (R&R) can be found on Grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization.

For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are called for.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

4.5.1.1 Concept Paper Narrative

The concept paper narrative is a word-processed document of no more than ten (10) single-spaced pages. Applicants must not include any classified information. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as "Proprietary" or "Sensitive Business Information" and provide an indication as to what specific information is proprietary or sensitive. Items 1) through 6) below must be completed and attached as a single document to Item 20. Pre-application on the SF-424 (R&R).

1) **Cover Sheet**. (The cover sheet does not contribute to the concept paper narrative page limit.) The cover sheet is a one-page document providing:
    a. NOFO Name and Reference Number (2025-NIST-CHIPS-AIAE-Sustainability-01)
    b. Concept paper submission date
    c. Proposal title
    d. Materials Classes and Applications (see Section 1.4.2)
    e. Name of the applicant organization
    f. Name of the project director(s)/principal investigator(s)
    g. Any major subrecipients or collaborating institutions (noting any ERIs)
    h. Point of contact for the applicant, to include the complete name, address, telephone number, and business e-mail address
    i. Total funds requested (rough order of magnitude)
    j. Period of performance start and end dates (estimated calendar year and quarter)

k. Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

2) **Concept Paper Quad Chart.** (Not to exceed one (1) page.) This does not contribute to the concept paper narrative page limit.) The Concept Paper Quad Chart is a one-page summary/abstract, suitable for dissemination to the public, identifying the name of the applicant, the principal investigator(s), the proposal title, the Materials Classes and Applications, Programmatic and Co-optimization Targets, and major participants. The Quad Chart must also state the problem addressed by and the potential impact of the project, consistent with the Relevance to Economic and National Security evaluation criteria. The Quad Chart must not include any classified information or proprietary or sensitive business information.

3) **Project Description.** A description of the proposed project covering each of the items listed below in sufficient detail to permit evaluation of the concept paper in accordance with the evaluation criteria (see Section 5.1).

   a. **Impact Statement.** Provide a clear problem statement and well-defined project outcomes, including each of the following aspects:
      i. A summary of the selected Materials Classes and Applications (see Section 1.4.2);
      ii. A summary of the Co-optimization Targets (Areas 1 – 4, see Section 1.4.3) and Programmatic Targets (Areas 5 – 7, see Section 1.4.4);
      iii. An explanation of how each of the above are relevant to industry needs, the CHIPS R&D mission and goals (see Section 1.1.1), and the objectives of this NOFO (see Section 1.1.2); and
      iv. An explanation of the project's Relevance to Economic and National Security, as expressed in the evaluation criteria (see Section 5.1).

   b. **Project Team Description.** As relevant to each Operational Area and noting capabilities anticipated to be provided by established research institutions, ERIs, industry, and other stakeholder organizations (e.g., civil society or labor organizations focused on environmental sustainability, or human health or safety), consistent with Section 1.4.6, provide a clear description of the roles, responsibilities, and capabilities of the applicant, as well as of any significant funded or unfunded collaborators, including each of the following aspects:
      i. **Applicant Capabilities.** Roles, responsibilities, capabilities, and expertise of the applicant that make it suitable to lead the project, including as relevant to:
         1. Managing research awards;
         2. Convening, roadmapping, and technology transfer (OA1);
         3. R&D relevant to AI/AE (OA2, see Section 1.4.6 and 1.5.2)
         4. Other research and innovation activities relevant to semiconductors and manufacturing sustainability; and
         5. EWD (OA3).

ii. **Collaborator Capabilities.** Roles, responsibilities, capabilities, and expertise of non-applicant members of the project team, particularly as relevant to:
    1. Convening, roadmapping, and technology transfer (OA1);
    2. R&D relevant to AI/AE (OA2, see Section 1.4.6 and 1.5.2)
    3. Other research and innovation activities relevant to semiconductors and manufacturing sustainability; and
    4. EWD (OA3).
iii. **Organizational Chart.** Provide an organizational chart showing the management structure for the collaboration and key management positions, as well as additional information describing:
    1. The roles and responsibilities for each position in the organizational chart;
    2. Reporting relationships among the positions in the organizational chart; and
    3. The names and roles of all key personnel who will contribute to the proposed project, including individuals not listed on the organizational chart.

The Project Team Description must be of sufficient detail to evaluate the project's Project Management, Resources, and Budget evaluation criteria (see Section 5.1). However, CHIPS R&D anticipates that identified collaborators and their roles and responsibilities may evolve and solidify over time, including between concept paper and full application, as applicable.

c. **Stakeholder Collaboration Strategy.** Provide an overview of the proposed strategies for engaging and developing the appropriate stakeholder community, including each of the following aspects:
    i. **Research Advisory Board Plan.** A detailed description of the expected composition and responsibilities of the Research Advisory Board, or of similar mechanisms to receive regular industry and other stakeholder guidance on relevant materials, AI/AE, or sustainability challenges. CHIPS R&D strongly recommends applicants to establish a Research Advisory Board, consisting of recognized leaders in the fields of AI/AE, semiconductor manufacturing, and sustainability, to help evaluate progress and to guide research directions; and
    ii. **CHIPS-funded Entity Collaboration Plan.** A description of planned collaborative partnerships with the CHIPS Manufacturing USA Institute, NSTC, or other CHIPS-funded entities, to advance potential innovations to higher TRLs.

d. **Research and Infrastructure Strategy.** Provide an overview of the project and an explanation of the project's Scientific and Technical Merit, as expressed in the evaluation criteria (see Section 5.1), including each of the following aspects:

i. **Co-Optimization Targets.** Details and rationale for the Co-optimization Targets (Themes 1 – 4, see Section 1.4.3), including why they represent a significant but achievable technological advance;
ii. **Research Capacity Programmatic Targets.** Details and rationale for the Research Capacity Programmatic Targets (Theme 5, see Section 1.4.4);
iii. **Roles and Responsibilities**. The roles and responsibilities of each member of the project team, relevant to achieving the above targets;
iv. **Project Phases and SMART Milestones.** Preliminary SMART Milestones for achieving each of the above targets—organized at approximately quarterly intervals and by project phase—suitable for go/revise/no-go checkpoints at each transition between project phases; and
v. **Physical Infrastructure Plan.** Consistent with Section 1.4.6, a preliminary description of the existing and planned equipment and infrastructure required to achieve the selected targets, including a table showing the expected physical location, ownership, and costs of such equipment and infrastructure. The Physical Infrastructure Plan should denote what physical infrastructure and equipment will be implemented at emerging research institutions, be made available to such institutions, and remain in operation at such institutions following the period of performance.

e. **Education and Workforce Development (EWD) Plan.** Consistent with Section 1.5.3 and the Education and Workforce Development evaluation criteria (see Section 5.1), describe the project's EWD approach. CHIPS R&D has provided an Education and Workforce Development Plan Guidebook to assist in the development of similar plans. The plan must address:
i. **EWD Programmatic Targets.** Details and rationale for the EWD Programmatic Target (Theme 6, see Section 1.4.4), including the targeted educational or professional levels and, if feasible, guided by a workforce needs assessment;
ii. **Roles and Responsibilities**. The roles and responsibilities of each member of the project team—such as accredited educational institutions, labor organizations, national laboratories, or other workforce training organizations—relevant to achieving the above targets;
iii. **Project Phases and SMART Milestones.** Preliminary SMART Milestones for achieving each of the above targets—organized at approximately quarterly intervals and by project phase—suitable for go/revise/no-go checkpoints at each transition between project phases; and
iv. **EWD Budget Estimate**. A rough order of magnitude estimate of funds set aside for EWD activities.

4) **Budget Estimate.** (This does not contribute to the concept paper narrative page limit.) Provide a rough order of magnitude estimate of the total project budget, including the lead applicant and any subrecipients.

5) **Letters of Commitment**. (This does not contribute to the concept paper narrative page limit.) As an appendix to the concept paper, provide a letter of commitment from each planned team member (including any subrecipients and unfunded collaborators) indicating their intention to participate and the capabilities they expect to provide to the proposed project. Each letter of commitment must not exceed two pages.

6) **Letters of Interest**. (Letters of interest do not contribute to the concept paper narrative page limit.) Letters of interest are optional and, where included, should indicate willingness from any third party to support this proposed effort. Letters of interest should outline the nature and importance of the collaboration or involvement being offered. Letters of interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests.

4.5.2 Concept Paper Format and Guidelines

Table 3. Concept Paper Format and Guidelines

Paper, Email, and Facsimile (fax) Submissions	Will not be accepted. All submissions must be submitted electronically via Grants.gov.
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be in landscape orientation.
Font	Use one of the following fonts: • Preferred: Calibri at a font size of 11 points or larger; • Acceptable alternatives: o Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger; o Times New Roman at a font size of 11 points or larger; or o Computer Modern family of fonts at a font size of 11 points or larger.
Line spacing	Single.
Page margins	One (1) inch top, bottom, left, and right.
Page layout	Portrait orientation only except for figures, graphs, images, and pictures.
Page limit	Ten (10) pages for concept paper narrative.
Page limit includes	Concept paper narrative, including the Project Description (Impact Statement, Project Team Description, Stakeholder Collaboration

	Strategy, Research and Infrastructure Strategy, Education and Workforce Development Plan), and any figures, graphs, images, and pictures.
Page limit excludes	Cover Sheet, Quad Chart, Budget Estimate, Letters of Commitment, Letters of Interest.
Page numbering	Number all pages sequentially.
Paper size	21.6 cm by 27.9 cm (8½ inches by 11 inches) with 2.5 cm (1 inch) margins.
Application language	English.
Typed document	All applications, including forms, must be typed.

4.6 FULL APPLICATION INSTRUCTIONS

Full applications will be accepted only from applicants that are invited after the concept paper stage. Submissions received from entities other than those specifically invited to submit a full application will not be reviewed or considered.

The required content and form of full applications submitted pursuant to this NOFO are set forth below.

4.6.1 Required Forms and Documents

The full application must contain the following:

4.6.1.1 Standard Form (SF)-424 (R&R), Application for Federal Assistance

The SF-424 (R&R) must be signed by an authorized representative of the applicant organization. For SF-424 (R&R), Items 5, 14, and 19, use the Zip Code + 4 format (##### - ####) when addresses are requested.

The list of certifications and assurances referenced in Item 17 of the SF-424 (R&R) is contained in the Federal Financial Assistance Certifications and Representations (Certs and Reps) as part of the SAM.gov entity registration.

SF-424 (R&R), Item 18. If the SF-LLL, Disclosure of Lobbying Activities form (see Section 4.6.1.5 below) is applicable, attach it to field 18.

Instructions for completing the SF-424 (R&R) can be found on Grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related(R&R) Application Package Guidance.

4.6.1.2 Research & Related Budget (Total Fed + Non-Fed)

The budget must reflect anticipated expenses for the full term of the proposed project, considering all potential cost increases, including cost of living adjustments.

The budget must be detailed in these categories:

A. Senior/Key Personnel;
B. Other Personnel;
C. Equipment Description;
D. Travel;
E. Participant/Trainee Support Costs;
F. Other Direct Costs;
G. Direct Costs (automatically generated);
H. Indirect Costs;
I. Total Direct and Indirect Costs (automatically generated);
J. Fee (not relevant to this competition);
K. Total Costs and Fee (automatically generated);
L. Budget Narrative and Justification document (item 4.6.1.8 below) must be attached to field L.

A separate detailed R&R Budget must be completed for each project phase during the proposed award. To add additional phases, click "Add Period" embedded at the end of the form. Information regarding the Research & Related Budget (Total Fed + Non-Fed) is available in the R&R Family Section of Grants.gov, as well as at the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.3 CD-511, Certification Regarding Lobbying

Enter "2025-NIST-CHIPS-AIAE-Sustainability-01" in the Award Number field. Enter the title of the application, or an abbreviation of that title, in the Project Name field.

4.6.1.4 Research and Related Other Project Information

Answer the highlighted questions and use this form to attach the Project Narrative (item 4 below), the Indirect Cost Rate Agreement (item 4.6.1.9), the Letters of Commitment and Interest, if applicable, (item 4.6.1.11 below), the Data Management Plan (item 4.6.1.12 below), and the Current and Pending Support Form (item 4.6.1.13 below). Instructions for completing the Research and Related Other Project Information form can be found in the Grants.gov R&R Forms Repository by scrolling down to Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Financial Assistance Agreement Management Office SF-424 Research & Related (R&R) Application Package Guidance. Research And Related Other Project Information and clicking the Instructions link, as well as in the NIST Financial Assistance Agreements Management Office SF-424 Research & Related (R&R) Application Package Guidance.

4.6.1.5 SF-LLL, Disclosure of Lobbying Activities

Complete this form if applicable.

4.6.1.6 Project Narrative

The project narrative is a word-processed document of no more than twenty (20) pages (single-spaced), which is responsive to the program description and the evaluation criteria described in this NOFO. The project narrative for the full application must contain the following information and required elements:

1) **Cover Sheet.** (Not to exceed one (1) page. This does not contribute to the project narrative page limit.) The cover sheet is a one-page document providing:
    a. NOFO Name and Reference Number (2025-NIST-CHIPS-AIAE-Sustainability-01)
    b. Full application submission date
    c. Proposal title
    d. Materials Classes and Applications (see Section 1.4.2)
    e. Name of the applicant organization
    f. Name of the project director(s)/principal investigator(s)
    g. Any major subrecipients or collaborating institutions (noting any ERIs)
    h. Point of contact for the applicant, to include the complete name, address, telephone number, and business e-mail address
    i. Total funds requested
    j. Period of performance start and end dates (estimated calendar year and quarter)
    k. Any statement regarding confidentiality, including proprietary or sensitive business information, if applicable

2) **Executive Summary and Quad Chart.** (Not to exceed three (3) pages. This does not contribute to the project narrative page limit.) The Quad Chart is a one-page abstract, suitable for dissemination to the public, identifying the name of the applicant, the principal investigator(s), the proposal title, the Materials Classes and Applications, Programmatic and Co-optimization Targets, and major participants. The Quad Chart must also state the problem addressed by and the potential impact of the project, consistent with the Relevance to Economic and National Security evaluation criteria. In addition to the Quad Chart, applicants may include an Executive Summary of the effort, also suitable for dissemination to the public, providing a concise summary of the proposed effort. The Executive Summary and Quad Chart must not include any classified information or proprietary or sensitive business information, as CHIPS R&D may make it available to the public after awards are issued.

3) **Table of Contents**. (This does not contribute to the project narrative page limit.)

4) **Project Description.** A description of the proposed project covering each of the items below and sufficient to permit evaluation of the application in accordance with the evaluation criteria (see Section 5.3). The project description must not include any classified information. Applicants must clearly identify proprietary information in their project description. Submissions containing proprietary or sensitive business information must have the cover page and each page containing such information clearly marked with a label such as "Proprietary" or "Sensitive Business Information" and provide an indication as to what specific information is proprietary or sensitive.

    a. **Impact Statement.** Provide a clear problem statement and well-defined project outcomes, including each of the following aspects:
        i. A summary of the selected Materials Classes and Applications (see Section 1.4.2.);
        ii. A summary of the Co-optimization Targets (Themes 1 – 4, see Section 1.4.3) and Programmatic Targets (Themes 5 – 7, see Section 1.4.4);
        iii. An explanation of how each of the above are relevant to industry needs and to the CHIPS R&D mission and goals (see Section 1.1.1) and the objectives of this NOFO (see Section 1.1.2);
        iv. If applicable, evidence of known or expected impacts to the U.S. Department of Defense, other government systems, critical infrastructure, and/or to advancing domestic production; and
        v. An explanation of the project's relevance to economic and national security, as expressed in the evaluation criteria (see Section 5.3).

    b. **Project Team Description.** As relevant to each Operational Area and noting capabilities provided by established research institutions, ERIs, industry, and other stakeholder organizations (e.g., civil society or labor organizations focused on environmental sustainability, or human health or safety), consistent with Section 1.4.6, provide a clear description of the roles, responsibilities, and capabilities of the applicant as well as of any significant funded or unfunded collaborators, including each of the following aspects:
        i. **Applicant Capabilities.** Roles, responsibilities, capabilities, and expertise of the applicant that make it suitable to lead the project, including as relevant to:
            1. Managing research awards;
            2. Convening, roadmapping, and technology transfer (OA1);
            3. R&D relevant to AI/AE (OA2, see Section 1.4.6 and 1.5.2)
            4. Other research and innovation activities relevant to semiconductors and manufacturing sustainability; and
            5. EWD (OA3).
        ii. **Collaborator Capabilities.** Roles, responsibilities, capabilities, and expertise of the non-applicant project team members, particularly as relevant to:
            1. Convening, roadmapping, and technology transfer (OA1);
            2. R&D relevant to AI/AE (OA2, see Section 1.4.6 and 1.5.2)

3. Other research and innovation activities relevant to semiconductors and manufacturing sustainability; and
4. EWD (OA3).

iii. **Organizational Chart.** Provide an organizational chart showing the management structure for the collaboration and key management positions, as well as additional information describing:
   1. The roles and responsibilities for each position in the organizational chart;
   2. Reporting relationships among the positions in the organizational chart; and
   3. The names and roles of all key personnel who will contribute to the proposed project, including individuals not listed on the organizational chart.

iv. **Foreign Partner Justifications**. Identify any foreign partners and, consistent for Section 3.1.4, the justification for their participation. Foreign partners may participate as members of a project team, as subrecipients or contractors, provided that they are not a foreign entity of concern, subject to CHIPS R&D review and approval.

The Project Team Description must be of sufficient detail to evaluate the project management, resources, and budget evaluation criteria (see Section 5.3).

c. **Stakeholder Collaboration Strategy.** Provide an overview of the proposed strategies for engaging and developing the appropriate stakeholder community, including each of the following aspects:

i. **Research Advisory Board Plan.** A detailed description of the expected composition and responsibilities of the Research Advisory Board, or of similar mechanisms to receive regular industry and other stakeholder guidance on relevant materials, AI/AE, or sustainability challenges;

ii. **CHIPS-funded Entity Collaboration Plan.** A description of planned collaborative partnerships with the CHIPS Manufacturing USA Institute, NSTC, or other CHIPS-funded entities, to advance potential innovations to higher TRLs; and

iii. **Commercial Viability and Domestic Production Plan (CVDP).** A written plan describing potential pathways to transition CHIPS-funded innovations to commercial viability and domestic production, where applicable, considering factors such as cost competitiveness, value proposition, and the impact of competitor products. CHIPS R&D has provided a Commercial Viability and Domestic Production Guide to assist in the development of similar plans. Where feasible, the plan should address topics relevant to:
   1. market analysis and competitor identification;

2. customer analysis, including perceived barriers to market penetration and any mitigations;
3. if relevant, plans for a sustainable business relevant to the funded innovation;
4. if relevant, commitments from partners to advance potential innovations to higher TRLs;
5. if relevant, the potential for domestic production and manufacturing scale-up of the funded innovation;
6. if relevant, any known factors requiring production of the funded innovation outside of the United States, as detailed in Section 2.6.2; and
7. if relevant, collaborative partnerships with government agencies, industry partners, research institutions, and standards bodies, as required to promote knowledge sharing or consensus building to support the adoption of innovations funded under this NOFO.

Given this NOFO's focus on industry-informed, university-based collaborations, certain CVDP elements (e.g., detailed marketability assessments) may be deferred until Phase 1 of the award. In lieu of these elements, CHIPS R&D strongly recommends that the applicant provide letters of interests or letters of commitment demonstrating private sector support for the proposed research outputs.

iv. **Intellectual Property Rights Management Plan (IPRM).** (Not to exceed five (5) pages. This does not contribute to the project narrative page limit.) A written plan that describes—

1. Any known (1) pre-existing IP (which may include patents, proprietary information, etc.) that will be used in completing the project, (2) IP that may be developed with funding under this NOFO, and (3) paths through which current and future project team members may access the above IP;
2. Any known expected training data and previously developed trained or untrained models expected to be used in the conduct of CHIPS-funded research, as well as the potential limitations on use or commercialization of the resulting research outputs;
3. How the applicant plans to manage IP that may be developed as a result of CHIPS-funded R&D, including provisions for Foreground IP, Background IP, commercial and non-commercial licensing of IP, data sharing, and publication;
4. The proposed management and ownership of IP and any existing or planned protocols to ensure domestic control and domestic production of CHIPS R&D-funded intellectual property, including to protect such IP (which may include

software) from foreign adversaries, pursuant to 15 U.S.C. § 4656(g) and Section 2.6;

5. Any desired deviations from applicable regulations and award terms, such as 2 C.F.R. § 200.315.

d. **Research and Infrastructure Strategy.** Provide an overview of the project and an explanation of the project's Scientific and Technical Merit, as expressed in the evaluation criteria (see Section 5.3), including each of the following aspects:
    i. **Co-optimization Targets.** Details and rationale for the Co-optimization Targets (Theme 1 – 4, see Section 1.4.3), including why they represent a significant but achievable technological advance;
    ii. **Research Capacity Programmatic Targets.** Details and rationale for the Research Capacity Programmatic Targets (Theme 5, see Section 1.4.4);
    iii. **Roles and Responsibilities**. The roles and responsibilities of each member of the project team, relevant to achieving the above targets;
    iv. **Project Phases and SMART Milestones.** SMART Milestones for achieving each of the above targets—organized at approximately quarterly intervals and by project phase—suitable for go/revise/no-go checkpoints at each transition between project phases;
    v. **Physical Infrastructure Plan.** Consistent with Section 1.4.6 a detailed description of how the applicant will develop, acquire, manage, operate, and provide access to research equipment and infrastructure, including computational capabilities, and expertise to achieve the selected targets, including a table showing the expected physical location, ownership, and cost of such equipment, infrastructure, and expertise. The Physical Infrastructure Plan should denote what physical infrastructure and equipment will be implemented at emerging research institutions, be made available to such institutions, and remain in operation at such institutions following the period of performance; and
    v. **Faculty Development Plan**. Consistent with Section 1.4.6, a detailed description of and commitment to project activities that will contribute to building a critical mass of faculty to expand and maintain research capacity, including but not necessarily limited to faculty at emerging research institutions.

e. **Education and Workforce Development (EWD) Plan.** Consistent with Section 1.5.3 and the Education and Workforce Development evaluation criteria (see Section 5.3), describe the project's EWD approach. CHIPS R&D has provided an Education and Workforce Development Plan Guidebook to assist in the development of similar plans. The plan must address:
    i. **EWD Programmatic Targets.** Details and rationale for the EWD Programmatic Target (Theme 6, see Section 1.4.4), including the

targeted educational or professional levels and, if feasible, guided by a workforce needs assessment;

ii. **Roles and Responsibilities**. The roles and responsibilities of each member of the project team—such as accredited educational institutions, labor organizations, national laboratories, or other workforce training organizations—relevant to achieving the above targets;

iii. **Proven, Industry-Relevant Training.** A description of the student training and support mechanisms (e.g., internships, research assistantships) and evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed in the programs and available jobs or to industry-recognized credentials or certifications. (Other evidence may include letters of interest from potential employers and labor organizations);

iv. **Project Phases and SMART Milestones.** SMART Milestones (e.g., number of students graduated and/or hired) for achieving each of the above targets—organized at approximately quarterly intervals and by project phase—suitable for go/revise/no-go checkpoints at each transition between project phases;

v. **EWD Infrastructure and Curriculum Plan.** A detailed description of any physical or virtual infrastructure that will be made available to support EWD training programs, including research infrastructure. If applicable, the applicant must further describe any new or modified curricula that will be developed or deployed to achieve the EWD Programmatic targets;

vi. **Recruitment and Retention Information.** A description of efforts to maximize access to and participation in the semiconductor workforce, including efforts to attract and retain a diverse student and trainee population such as supportive services and outreach to underserved communities; and

vii. **EWD Budget**. A description of the amount of funds set aside for EWD activities, by project phase.

f. **Broader Impacts Statement**. Consistent with Section 1.7, provide an overview of the proposed project's broader impacts, such as commitments to future investment, creating inclusive opportunities, environmental responsibility, or community impact and support.

i. If relevant, identify impacts on a new or existing community-based organization or alignment with regional, state, or local economic development strategies, assets, resources, or capacities;

ii. If relevant, identify any known or potential collaborations across the semiconductor industry or IP rights or licensing plan; and

iii. If relevant, identify potential private sector partners indicating interest in the funded innovation and the potential for industry to rapidly move

funded innovations, if successfully demonstrated, to higher TRL levels.

g. **Fundamental Research Declaration.** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.) Identify which of the proposed research activities, if any, the applicant believes NIST/CHIPS R&D should consider as fundamental research and the rationale for that determination. For any proposed fundamental research, identify the relevant project team member(s) to be involved. NIST/CHIPS R&D reserves sole discretion to determine which elements of a proposed research project shall be considered fundamental research.

h. **Research Security Plan**. (Not to exceed five (5) pages. This does not contribute to the project narrative page limit.) Provide a written plan that–
   i. Provides a point of contact on research security issues within the project leadership team;
   ii. Describes, as applicable, any internal processes or procedures to address foreign talent recruitment programs, conflicts of commitment, conflicts of interest, research security training, and research integrity;
   iii. Describes measures taken to ensure that appropriate practices for cybersecurity, such as the NIST Cybersecurity Framework and Cybersecurity and Infrastructure Security Agency (CISA) Cybersecurity Performance Goals (CPGs), are incorporated in the project;[l]
   iv. Lists any relevant certifications in place or plans to obtain such certifications (e.g., FCL, CMMC) and standards they follow (e.g. ISO/IEC 27001, ISO 8000-51); and
   v. For "covered institutions", describes the applicant's intent to establish and operate a Research Security Program.

i. **Gantt Chart/Timeline**. (This does not contribute to the project narrative limit.) Provide a Gantt Chart/timeline showing progress towards demonstrating the Co-optimization Targets and achievement of the Programmatic Targets, with corresponding SMART Milestones.

j. **Table of Abbreviations and Acronyms**. (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.) Provide an alphabetical list of all abbreviations, acronyms, and their meanings used in the full application.

[l] The CISA performance goals provide a baseline set of cybersecurity practices that are broadly applicable, with known risk-reduction value. They also allow applicants the ability to measure and improve their cybersecurity maturity, and a combination of recommended practices for IT and OT owners, including a prioritized set of security practices.

k. **Bibliographic List of References**. (Not to exceed five (5) pages. This does not contribute to the project narrative page limit.) Provide a complete bibliographic list of all references used within the application.

l. **Compliance Matrix.** (Not to exceed two (2) pages. This does not contribute to the project narrative page limit.) Applicants shall provide a compliance matrix in table format that explains how and where each evaluation criterion is addressed (see Section 5.3 for evaluation criteria). The table's format is at the discretion of the applicant.

m. **Table of Funded Participants and Unfunded Collaborators.** (This does not contribute to the project narrative page limit.) A table that identifies all organizations that will participate in and collaborate with the awarded team, known at the time of the application submission. The table should consist of an alphabetically ordered list, by organization, of all team members, funded and unfunded, including any known contractors. Foreign partners should be identified.

n. **Foreign Partner/Activity Justifications.** (This does not contribute to the project narrative page limit.) Applicants should provide concise initial justifications for the proposed involvement of any foreign partners or proposed execution of research activities overseas, consistent with Section 3.1.4).

o. **Written Summary of Certain Research Partnerships and Technology Transfer Commitments.** (This does not contribute to the project narrative page limit.) Applicants should provide a written summary that describes any research partnerships or technology transfer commitments in areas relevant to the activities within this NOFO or any other areas related to the mission and goals of CHIPS R&D (see Section 1.1.1) between the applicant entity and (a) any entities located in a foreign country of concern or (b) with any entities that are foreign entities of concern;[m] each foreign entity should be identified.

4.6.1.7 Resume(s) or CV(s)

Resumes or CVs must not exceed two (2) pages per individual, and do not contribute to the project narrative page limit. Resumes or CVs are required for all key personnel, including the principal investigator(s) and anyone deemed a "covered individual" per Section 2.5.4 of this NOFO. For purposes of research security reviews, any individual whose resume or CV is included will be deemed a covered individual. The resumes or CVs should highlight experience relevant to the proposed work and should provide sufficient detail for CHIPS R&D to make determinations regarding covered individuals in accordance with 42 U.S.C. § 6605.

4.6.1.8 Budget Narrative and Justification

The budget narrative and justification must not exceed five (5) pages. These materials do not contribute to the project narrative page limit. There is no required format for the budget narrative and justification; however, the written justification must include the necessity and the basis for the cost, as described below. Proposed funding levels must be consistent with the project scope, and only allowable costs must be included in the budget.

The proposed budget will be evaluated in accordance with the evaluation criteria for Project Management, Resources, and Budget. Applicants must provide a detailed budget table[n] and budget narrative.[o] Budget tables will be reviewed to determine if all costs are allowable in accordance with Section 3.3 of this NOFO.

Information required for each budget category is as follows (categories not listed are automatically generated by the form or are not relevant to this competition):

A. **Senior/Key Personnel** – At a minimum, the budget justification must include the following: name, job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the individual on the proposed project and the work to be performed.

   Senior/Key Person Fringe Benefits – Fringe benefits must be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking) must not be charged under another cost category.

B. **Other Personnel** – Data is requested at the project role level, and not at the individual level for Other Personnel. The budget justification must include the following: job title, commitment of effort on the proposed project in terms of average number of hours per week or percentage of time, salary rate, total direct charges on the proposed project, description of the role of the position on the proposed project and the work to be performed.

   Other Personnel Fringe Benefits – Fringe benefits must be identified separately from salaries and wages and based on rates determined by organizational policy. The items included in the fringe benefit rate (e.g., health insurance, parking) must not be charged under another cost category.

[n] A budget table shows accounting information broken out by budget form object class categories in rows and summarized by project phase and Federal award total in the columns.
[o] The budget should reflect the total costs, composed of both the Federal funds that will be requested and the co-investment that is planned as appropriate.

C. **Equipment Description** – Equipment is defined as an item of property that has an acquisition cost of $10,000 or more (unless the organization has established lower levels) and an expected service life of more than one year. The budget justification must list each piece of equipment, the cost, and a description of how it will be used and why it is necessary to the successful completion of the proposed project. Please note that any general use equipment (computers, etc.) charged directly to the award must be allocated to the award according to expected usage on the project. Any items that do not meet the threshold for equipment can be included under the Materials and Supplies line item in Section F, Other Direct Costs (see below).

D. **Travel** – For all travel costs required by the applicant to complete the project, including attendance at any relevant conferences and/or meetings, the budget justification for travel must include the following: destination; names or number of people traveling; dates and/or duration; mode of transportation, lodging and subsistence rates; and description of how the travel is directly related to the proposed project. For travel that is yet to be determined, please provide best estimates based on prior experience. If a destination is not known, an approximate amount may be used with the assumptions given for the location of the meeting. Applicants should build into travel budgets anticipated travel and related costs for planned team meetings.

E. **Participant/Trainee Support Costs** – Participant support costs are stipends, subsistence allowances, travel, and registration fees paid to or on behalf of participants or trainees, who are not employees of your organization, for conferences or training projects. The budget justification must indicate the names or number of participants or trainees, a description and calculation of costs per person, a description and date of the event, and a description of why the cost is necessary for the successful completion of the proposed project.

F. **Other Direct Costs** – For costs that do not easily fit into the other cost categories, please list the cost, and the breakdown of the total costs by quantity or unit of cost. Include the necessity of the cost for the completion of the proposed project. Only allowable costs can be charged to the award. Each subaward must be treated as a separate item in the Other Direct Costs category. Describe the services to be provided and the necessity of the subaward to the successful performance of the proposed project. Subrecipients perform part of the project scope of work. For each subaward, applicants must provide budget detail justifying the cost of the work performed on the project.

H. **Indirect Costs** – Commonly referred to as Facilities & Administrative (F&A) Costs, indirect costs are defined as costs incurred by the applicant organization that cannot otherwise be directly assigned or attributed to a specific project. For more details, see Section 4.6.1.9 of this NOFO.

4.6.1.9 Indirect Cost Rate Agreement

If indirect costs are included in the proposed budget, provide a copy of the approved negotiated agreement if this rate was negotiated with a cognizant Federal audit agency. If the rate was not established by a cognizant Federal audit agency provide a statement to this effect. If the successful applicant includes indirect costs in the budget and has not established an indirect cost rate with a cognizant Federal audit agency, the applicant may be required to obtain such a rate upon award.

Alternatively, applicants that do not have a current negotiated (including provisional) indirect cost rate may elect to charge a de minimis rate of fifteen (15) percent of modified total direct costs (MTDC). Applicants proposing a fifteen (15) percent de minimis rate must note this election as part of the budget portion of the application.

4.6.1.10 Subaward Budget Form

The Research & Related Subaward Budget Attachment Form is required if subrecipients are included in the application budget.

Instructions for completing subaward budget forms are available by visiting the R & R Family section of the Grants.gov Forms Repository and scrolling down to the R & R Subaward Budget Attachment(s) Form and selecting "Instructions."

4.6.1.11 Letters of Commitment and Interest

1. **Letters of Commitment** – (Letters of Commitment do not apply to the project narrative page limit.) Letters that commit specific resources or funding to the proposed project – in the event that the application is funded – are required from all of the following that apply.
   - If the application includes any subawards to identified third parties, a letter of commitment from an authorized representative of each proposed organization (such as the appropriate dean of an emerging research institution) must be included. Each letter must verify the organization's willingness to participate as a subrecipient, as applicable, and describe the work they would do in relation to the Project Narrative.
   - Letters of commitment from subrecipients that are operators of an FFRDC (see Section 3.1.1) or are Federal entities must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and documentation from the FFRDC's sponsoring institution citing the FFRDC's eligibility to participate in competitive Government funding opportunities, the FFRDC's compliance with the sponsor agreement, and confirmation from the sponsoring agency that they can receive Federal funds from NIST.
   - Letters of commitment from subrecipients that are Federal entities (see Section 3.1.2) must include, in addition to the information above, documentation demonstrating that the proposed work does not compete with the private sector and/or citing the specific statutory authority and contractual authority, if relevant, establishing their ability to receive Federal award funds and compete with industry.

- If key personnel who are willing to fill vacancies on the applicant's or subrecipient's staff are identified by the applicant, a letter of commitment from each of the relevant key-personnel individuals must be included. The letter from each such individual, or group of individuals, should indicate the relationship of the writer to the applicant and how the writer will help fulfill the efforts described in the Funding Opportunity Description (see Section 1.4).
- Applicant and Third-Party Non-Federal Co-investment: Letters of commitment for all sources of non-Federal co-investment may be included.
    - Applicant Non-Federal Co-investment (Cash and In-kind): As appropriate, a letter of commitment is required from an authorized representative of the applicant, stating the total amount of co-investment to be contributed by the applicant towards the proposed team. This letter includes a per year break-out of cash co-investment and in-kind (non-cash) contributions for the duration of the award. Given this NOFO's focus on industry-informed, university-based collaborations, CHIPS R&D welcomes but does not necessarily anticipate applicant non-Federal co-investment.
    - Third Party Co-investment (Cash and In-kind): As appropriate, the applicant must include a letter of commitment from an authorized representative of each third-party organization providing cash or in-kind contributions that are being committed to the proposed project, subject to the application being funded. Any such letter(s) should clearly state: whether the third-party contribution will consist of cash contributions, in-kind contributions, or a combination thereof; the total amount or value of the contribution, including a break-out of cash versus in-kind contributions (as applicable); the time period over which the third-party contribution will be made; any interim performance requirements for phased contributions; and all contingencies or pre-conditions to which the contribution is subject.
    - Letters of commitment should not be letters submitted by non-proposing entities wishing to vouch for the applicant's (or entities associated with the applicant) knowledge, skills, and abilities or entities to conduct the proposed work. These letters should be in the form of a letter of interest. Letters of Commitment from education and workforce development partners should describe the specific role of the partner.

2) **Letters of Interest** – (Letters of Interest do not apply to the project narrative page limit). Letters of Interest are optional and, where included, should indicate willingness from any third party to support the proposed effort. Letters of Interest should outline the nature and importance of the collaboration or involvement being offered. Letters of interest may also be from non-proposing entities wishing to vouch for the applicant's knowledge, skills, or abilities to conduct the proposed work or to express interest as potential customers for or users of the technologies to be developed under the project plan, including those with commercial, national security, or critical infrastructure interests.

4.6.1.12 Data Management Plan

The Data Management Plan (DMP) does not apply to the project narrative page limit. Consistent with NIST Policy 5700.00[p], Managing Public Access to Results of Federally Funded Research, and NIST Order 5701.00[q], Managing Public Access to Results of Federally Funded Research," applicants must include a DMP.

All applications for activities that will generate scientific data using CHIPS R&D funding are required to adhere to a DMP or explain why data sharing and/or preservation are not within the scope of the proposed project. For the purposes of the DMP, NIST adopted the definition of "research data" at 2 C.F.R. § 200.315(e)(3).

The DMP must include, at a minimum, a summary of proposed activities that are expected to generate data; a summary of the types of data expected to be generated by the identified activities; a plan for storage and maintenance of the data expected to be generated by the identified activities, including after the end of the award's period of performance; and a plan describing whether and how data generated by the identified activities will be reviewed and made available to the public.

A template for the DMP, an example DMP, and the rubric against which the DMP will be evaluated for sufficiency are available online at Data Management Plan Template, Example, and Rubric. An applicant is not required to use the template as long as the DMP contains the required information.

If an application stands a reasonable chance of being funded and the DMP is determined during the review process to be insufficient, the program office may reach out to the applicant to resolve deficiencies in the DMP. If an award is issued prior to the deficiencies being fully rectified, the award will include a term and condition stating that no research activities shall be initiated, or costs incurred for those activities, under the award until the NIST Agreements Officer amends the award to indicate the term and condition has been satisfied. Reasonable costs for data preservation and access may be included in the application.

4.6.1.13 Current and Pending Support Form

Applicants must identify all sources of current and potential funding, including this award, for all covered individuals. Any current project support (e.g., Federal, state, local, public or private foundations, etc.) must be listed on this form. The proposed project and all other projects or activities requiring a portion of time of the Principal Investigator(s) (PI), co-PI (s), and key personnel must be included, even if no salary support is received. The total award amount for the entire award period covered, including indirect costs, must be shown, as well as the number of person-months per year to be devoted to the project, regardless of the source of support. Similar

[p] https://www.nist.gov/system/files/documents/2018/06/19/final_p_5700.pdf
[q] https://www.nist.gov/system/files/documents/2019/11/08/final_o_5701_ver_2.pdf

information must be provided for all proposals already submitted or that are being submitted concurrently to other potential funders.

Applicants must complete the Current and Pending Support Form, using multiple forms as necessary to account for all activity for each covered individual. A separate form must be used for each identified individual.

Applicants must download the Current and Pending Support Form from the NIST website and reference the guidance provided as it contains information to assist with accurately completing the form.

4.6.2 Attachment of Required Documents

Items 4.6.1.1 through 4.6.1.4 above are part of the standard application package in Grants.gov and can be completed through the download application process.

Item 4.6.1.5 the SF-LLL, Disclosure of Lobbying Activities form, is an optional application form which is part of the standard application package in Grants.gov. If item IV.2.a.(5), the Form SF-LLL, Disclosure of Lobbying Activities, is applicable to the proposal, attach it to field 18 of the SF-424 (R&R), Application for Federal Assistance.

Item 4.6.1.6, the Project Narrative, must be attached to field 8 (Project Narrative) of the Research and Related Other Project Information form by clicking on "Add Attachment."

Item 4.6.1.8, the Budget Narrative and Justification, must be attached to field L (Budget Justification) of the Research and Related Budget (Total Fed + Total Non-Fed) form by clicking on "Add Attachment."

Items 4.6.1.7, Resume(s) or CV(s), 4.6.1.7, the Indirect Cost Rate Agreement, 4.6.1.9 Letters of Commitment if applicable to the submission, 4.6.1.12, the Data Management Plan, 4.6.1.13, the Current and Pending Support Form must be completed and attached by clicking on "Add Attachments" found in item 12 (Other Attachments) of the Research and Related Other Project Information form.

Item 4.6.1.10, the Subaward Budget Form(s), if applicable to the submission, must be attached to the Research & Related Subaward Budget (Total Fed + Non-Fed) Attachment(s) Form in the application package.

Following these directions will create zip files which permit transmittal of the documents electronically via Grants.gov.

Applicants must carefully follow specific Grants.gov instructions to ensure the attachments will be accepted by the Grants.gov system. A receipt from Grants.gov indicates only that an application was transferred to the system. It does not provide details concerning whether all attachments (or how many attachments) transferred successfully. An applicant will receive a

series of e-mail messages over a period of up to two business days before learning whether a Federal agency's electronic system received its application.

Applicants are strongly advised to access the "Download Submitted Forms and Applications" option at Grants.gov to check if all attachments were contained in their submitted application and to download a zip file of the complete submitted application for their records.

After submitting an application, the applicant may check the status of its application by using the: CHECK APPLICATION STATUS instructions on Grants.gov. If any, or all, of the required attachments are absent from the submission, follow the attachment directions, resubmit the application, and check again for the presence of the required attachments.

If the directions found at the Grants.gov Get Started help page are not effective, please contact the Grants.gov Help Desk immediately. If calling from within the United States or from a U.S. territory, please call 800-518-4726. If calling from outside the United States or from a U.S. territory, please call 606-545-5035. Questions also may be e-mailed to support@grants.gov. Assistance from the Grants.gov Help Desk will be available around the clock every day, with the exception of Federal holidays. Help Desk service will resume at 7:00 a.m. Eastern Time the day after Federal holidays.

Please be advised that it can take up to two business days for an application to fully move through the Grants.gov system to CHIPS R&D.

CHIPS R&D uses the Tracking Numbers assigned by Grants.gov and does not issue Agency Tracking Numbers.

4.6.3 Full Application Format and Guidelines

Table 4. Full Application Format and Guidelines

Paper, Email, and Facsimile (fax) Submissions	Will not be accepted. All applications must be submitted electronically through Grants.gov.
Figures, Graphs, Images, and Pictures	Should be of a size that is easily readable or viewable and may be displayed in landscape orientation. Any figures, graphs, images, or pictures count toward the page limit for the project narrative.

Font	Use one of the following fonts:
	• Preferred: Calibri at a font size of 11 points or larger
	• Alternatives:
	  ○ Arial (not Arial Narrow), Courier New, or Palatino Linotype at a font size of 10 points or larger;
	  ○ Times New Roman at a font size of 11 points or larger; or
	  ○ Computer Modern family of fonts at a font size of 11 points or larger

Project narrative page limit	The project narrative is limited to twenty (20) pages.
Project narrative page limit exclusions	Select materials required for the full application, which do not contribute to the 20-page limit of the project narrative, are listed below. Intellectual Property Rights Management (IPRM) (5-page limit) Foreign Partner/Activity Justifications Fundamental Research Declaration (2-page limit) Research Security plan (5-page limit) Gantt Chart/Timeline Table of Abbreviations and Acronyms (2-page limit) Bibliographic List of References (5-page limit) Compliance Matrix (2-page limit) Table of Funded Participants and Unfunded Collaborators
Other page limit exclusions	Additional materials required in the full application that are not subject to the project narrative page limit are listed below. SF-424 (R&R), Application for Federal Assistance Research & Related Budget (Total Fed + Non-Fed) CD-511, Certification Regarding Lobbying Research and Related Other Project Information SF-LLL, Disclosure of Lobbying Activities Cover Sheet (1-page limit) Executive Summary and Quad Chart (3-page limit) Table of Contents Resume(s) or CV(s) Budget Narrative and Justification Indirect Cost Rate Agreement Subaward Budget Form Letters of Commitment and/or Interest Data Management Plan Current and Pending Support Forms
Page layout	The project narrative must be in portrait orientation
Page size	21.6 centimeters by 27.9 centimeters (8½ inches by 11 inches) with 2.5-centimeter (1 inch) margins
Page numbering	Number all pages sequentially within each section of the application, in a format that is clear and consistent. CHIPS R&D suggests formatting such as ‘Project Narrative page 1 of 10’ for ease of reference
Application language	All documents must be in English, including but not limited to the initial application, any additional documents submitted in response to a CHIPS R&D request, all reports, and any correspondence with CHIPS R&D
Typed document	All applications, including forms, must be typed

4.7 APPLICATION REPLACEMENT PAGES

Applicants may not submit replacement pages and/or missing documents once a concept paper or full application has been submitted through Grants.gov. Any replacement pages or missing documents must be made by submission of a new concept paper or full application in its entirety that must be received by NIST by the submission deadline.

4.8 UNIQUE ENTITY IDENTIFIER AND SYSTEM FOR AWARD MANAGEMENT (SAM)

Pursuant to 2 C.F.R. part 25, an applicant is required to: (i) be registered in SAM (https://www.sam.gov) before submitting an application; (ii) provide a valid unique entity identifier (UEI) in its application; and (iii) continue to maintain an active SAM registration with current information at all times during which it has an active Federal award or an application or plan under consideration by a Federal awarding agency, unless otherwise excepted from these requirements pursuant to 2 C.F.R. § 25.110. For any entity that newly registers at https://www.sam.gov, the UEI will be assigned to that entity as part of the registration process.

Under this NOFO, NIST will not make a Federal award to any applicant until the applicant has fully complied with SAM registration requirements and, if an applicant has not fully complied with the requirements by the time that NIST is ready to make a Federal award pursuant to this NOFO, NIST may determine that the applicant is not qualified to receive a Federal award and may, in its sole discretion, make a Federal award to another applicant.

4.9 SUBMISSION DATES AND TIMES

CHIPS R&D strongly encourages applicants to begin the process of completing SAM registration as early as possible. While this process ordinarily may take between three days and two weeks, in some circumstances it can take six or more months to complete due to information verification requirements.

Applicants should be aware, and factor into their application submission planning, that the Grants.gov system closes periodically for routine maintenance. Applicants are encouraged to visit Grants.gov for information on any scheduled closures.

Please note that an award under this NOFO cannot be issued if the designated recipient's registration at SAM.gov is not active at the time of the award.

4.9.1 Concept Papers

Concept papers must be received electronically through Grants.gov no later than 11:59 p.m. Eastern Time, on January 13, 2025. CHIPS R&D will consider the date and time recorded by

Grants.gov as the official submission time of the applicant's concept paper. Concept papers received after the specified deadline will not be reviewed or considered.

Review of the concept papers, selection, and notification to applicants is expected to be completed on or about March 13, 2025. Any changes to the expected completion date will be communicated on the CHIPS R&D Frequently Asked Questions page.

4.9.2 Full Applications

The full application deadline will be communicated to invited applicants at the time of invitation. CHIPS R&D will consider the date and time recorded by Grants.gov as the official submission time of the applicant's application. Applications received after the specified deadline will not be reviewed or considered.

4.10 INTERGOVERNMENTAL REVIEW

Applications under this program are not subject to Executive Order 12372.

4.11 FUNDING RESTRICTIONS

Construction activities are not an allowable cost under this program. However, costs related to internal modifications of existing buildings that may be necessary to carry out the proposed research tasks may be allowed, as determined by NIST in its sole discretion.

In addition, recipients and subrecipients may not charge any profits, fees, or other increments above cost to an award issued pursuant to this NOFO.

5 APPLICATION REVIEW INFORMATION

5.1 CONCEPT PAPER EVALUATION CRITERIA

The CHIPS R&D merit review process will assess concept papers against the following five criteria: (1) relevance to economic and national security; (2) overall scientific and technical merit; (3) project management; (4) transition and impact strategy; and (5) education and workforce development. The first two criteria—relevance to economic and national security and the overall scientific and technical merit—will receive the greatest and approximately equal weight. The remaining three criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical. A concept paper will be recommended for full application only if CHIPS R&D determines that each criterion is adequately addressed in the application materials.

5.1.1 Relevance to economic and national security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving CHIPS R&D's mission and goals (see Section 1.1.1). Reviewers will therefore evaluate the extent to which the proposed project is likely to:

1) Advance long-lasting domestic semiconductor R&D capabilities (including physical infrastructure and cross-institution collaborations) relevant to AI/AE and to sustainable manufacturing, particularly at ERIs;
2) Support a more resilient and sustainable U.S. semiconductor manufacturing supply chain, such as by addressing the risks associated with geographic concentration of current semiconductor production; and
3) Generate substantial economic benefits to the Nation that extend beyond the direct return to funded project participants, including through the potential for industry adoption of the research outputs.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement**; **Research and Infrastructure Strategy**, including the **Physical Infrastructure Plan**; **Stakeholder Collaboration Strategy**, including the **Research Advisory Board Plan**; and **Letters of Commitment/Interest.**

5.1.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed project and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.2. Specifically, the proposal must be clear and concise and identify the materials classes and applications, co-optimization and Programmatic Targets, a detailed plan and rational approach to achieving those targets, and major technical hurdles, risks, and mitigations. Reviewers will therefore evaluate the extent to which the proposal:

(1) Describes activities that are innovative, original, or potentially transformative;
(2) Includes activities, goals, objectives, and strategies that are well-reasoned, well-organized, and presented in sufficient technical detail; and
(3) Demonstrates knowledge of the current state of the art in relevant fields and the feasibility of achieving proposed Co-optimization and Programmatic Targets, considering gaps, constraints, and significant challenges that must be addressed.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement** and **Research and Infrastructure Strategy**, including the **Project Phases and SMART Milestones** and **Physical Infrastructure Plan**.

5.1.3 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the proposed project. Applicants must demonstrate that they have the appropriate personnel and management structure to complete the work, access to the required equipment/facilities, and that the requested budget matches the need and is reasonable. Reviewers will therefore evaluate the extent to which the proposal:

(1) Identifies key staff, leadership, and technical experts (which may include partner personnel) with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;
(2) Identifies equipment, facilities, and other physical and computational capabilities required to support the project and convincingly demonstrates either current access to or a clear plan to obtain access to such equipment and facilities; and
(3) Demonstrates leadership and research participation from ERIs and lasting access to physical and computational capabilities for researchers from ERIs.

Relevant application materials include, but are not necessarily limited to, the **Budget Estimate**, **Stakeholder Collaboration Strategy**, and **Research and Infrastructure Strategy**, including the **Project Phases and SMART Milestones** and **Physical Infrastructure Plan**.

5.1.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will therefore evaluate the extent to which the proposal:

(1) Provides a reasonable approach for transitioning the proposed technology to commercial deployment.

Relevant application materials include, but are not necessarily limited to, the **Stakeholder Collaboration Strategy**, including the **Research Advisory Board Plan**, and **Letters of Commitment/Interest**. The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.1.5 Education and Workforce Development (EWD)

This criterion addresses the quality, completeness, rationality, and feasibility of the proposed project's EWD models and plans. Reviewers will therefore evaluate the extent to which the proposal:

(1) Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, and hired), appropriate to developing a diverse and skilled workforce.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement** and **Education and Workforce Development Plan.**

5.2 CONCEPT PAPER SELECTION FACTORS

The selection factors for concept papers in this competition are:

(1) Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings;

(2) Relevance to Program and Mission. Alignment with the objectives of this NOFO as well as the mission, goals, and priorities of the CHIPS R&D;
(3) Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources;
(4) Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, non-profit research organizations, etc.) in the overall CHIPS R&D portfolio; and
(5) Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, environmental responsibility, and regional economic development goals, including plans for broader impact consistent with Sections 1.5.3 and 1.7 of this NOFO.

5.3 FULL APPLICATION EVALUATION CRITERIA

The CHIPS R&D merit review will assess full applications against the following five criteria: (1) relevance to economic and national security; (2) overall scientific and technical merit; (3) project management, resources, and budget; (4) transition and impact strategy; and (5) education and workforce development. The first two criteria— relevance to economic and national security and the overall scientific and technical merit—will receive the greatest and approximately equal weight. The remaining three criteria will receive approximately equal weight to each other. The evaluation will be qualitative, not numerical. Applications will be recommended for award only if CHIPS R&D determines that each criterion is adequately addressed in the application materials.

5.3.1 Relevance to Economic and National Security

This criterion addresses relevance of the proposal to enhancing U.S. economic or national security competitiveness and to achieving CHIPS R&D's mission and goals (see Section 1.1.1). Specifically, the applicant must clearly demonstrate its plans and capabilities to enable domestic invention, development, prototyping, manufacture, and deployment of advanced packaging technologies. Reviewers will therefore evaluate the extent to which the proposed project is likely to:

(1) Advance long-lasting domestic semiconductor R&D capabilities (including physical infrastructure and cross-institution collaborations) relevant to AI/AE and to sustainable manufacturing, particularly at ERIs;
(2) Support a more resilient and sustainable U.S. semiconductor manufacturing supply chain, such as by addressing the risks associated with geographic concentration of current semiconductor production;
(3) Generate substantial economic benefits to the Nation that extend beyond the direct return to funded project participants, including through the potential for industry adoption of the research products; and
(4) Support the development of semiconductors necessary to the U.S. Department of Defense, other government systems, or critical infrastructure.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement**; **Research and Infrastructure Strategy**, including the **Physical Infrastructure Plan** and **Faculty Development Plan**; **Stakeholder Collaboration Strategy**, including the **Research Advisory Board Plan** and **CVDP**; and **Letters of Commitment/Interest.**

5.3.2 Overall Scientific and Technical Merit

This criterion addresses the quality, innovativeness, and feasibility of the proposed project and the potential for meeting the objectives of this NOFO, as expressed in Section 1.1.2. Specifically, the proposal must be clear and concise and identify the materials classes and applications, co-optimization and Programmatic Targets, a detailed plan and rational approach to achieving those targets, and major technical hurdles, risks, and mitigations. Reviewers will therefore evaluate the extent to which the proposal:

(1) Describes activities that are innovative, original, or potentially transformative;
(2) Includes activities, goals, objectives, and strategies that are well-reasoned, well-organized, and presented in sufficient technical detail;
(3) Demonstrates knowledge of the current state of the art in relevant fields and the feasibility of achieving proposed Co-Optimization and Programmatic Targets, considering gaps, constraints, and significant challenges that must be addressed; and
(4) Incorporates effective mechanisms to assess success, including meaningful SMART milestones and targets relevant to the selected Materials Classes and Applications and to each Operational Area.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement** and **Research and Infrastructure Strategy**, including the **Project Phases and SMART Milestones** and **Physical Infrastructure Plan**.

5.3.3 Project Management, Resources, and Budget

This criterion addresses the reasonableness, appropriateness, and cost-effectiveness of the proposed budget, management strategy, and resources, relative to the work and objectives of the proposed project. Applicants must demonstrate that they have the appropriate personnel and management structure to complete the work, access to the required equipment/facilities, and that the budget requested matches the need and is reasonable. Reviewers will therefore evaluate the extent to which the proposal:

(1) Provides a clear picture of annual expenditures and a budget that is cost-effective, reasonable, and consistent with the proposed scope of work;
(2) Clearly describes a project management approach that supports the objectives of this NOFO, including schedule and budget risk and mitigation strategies;
(3) Identifies key staff, leadership, and technical experts (which may include partner personnel) with qualifications and experience appropriate to the proposed work, including prior experience and results in efforts similar in nature, purpose, or scope of proposed activities;

(4) Identifies equipment, facilities, and other physical and computational capabilities required to support the project and convincingly demonstrates either current access to or a clear plan to obtain access to such equipment and facilities;
(5) Demonstrates leadership and research participation from ERIs and lasting access to physical and computational capabilities for researchers from ERIs;
(6) Describes mechanisms for meaningful and potentially long-lasting collaborations between stakeholders, including ERIs, other research institutions, industry, CHIPS-funded activities, and where appropriate, civil society organizations; and
(7) The availability of funding and the reasonableness and reliability of co- investment from specific, known, and anticipated non-Federal sources.

Relevant application materials include, but are not necessarily limited to, the **Budget Narrative**, **Stakeholder Collaboration Strategy**, and **Research and Infrastructure Strategy**, including the **Project Phases and SMART Milestones**, **Physical Infrastructure Plan**, and **Faculty Development Plan**.

5.3.4 Transition and Impact Strategy

This criterion addresses the project's potential for supporting the commercialization and domestic production of funded semiconductor innovations, as well as beneficial impacts to the broader domestic research, development, and innovation ecosystem. Reviewers will therefore evaluate the extent to which the proposal:

(1) Demonstrates an understanding of competing commercial and emerging semiconductor materials technologies and how proposed innovations could provide a significant, marketable improvement over these competing technologies, as applicable;
(2) Provides a reasonable approach for transitioning the proposed technology to commercial deployment;
(3) Demonstrates an intent to support or participate in other R&D programs and a credible commitment by relevant members of Project Team to future investment, creating inclusive opportunities, environmental responsibility, and community impact and support; and
(4) Describes the potential for the proposed work to contribute to domestic semiconductor R&D and manufacturing capability, such as contributions to the development of new or existing regional semiconductor industry clusters or plans to leverage or contribute to regional facilities, manufacturers, infrastructure, and suppliers.

Relevant application materials include, but are not necessarily limited to, the **Broader Impacts Statement**; **Stakeholder Collaboration Strategy**, including the **CVDP**; and **Letters of Commitment/Interest**. The evaluation may also consider the applicant's history of transitioning (or plans to transition) technologies to foreign governments or to companies that are foreign owned, controlled, or influenced.

5.3.5 Education and Workforce Development (EWD)

This criterion addresses the quality, completeness, rationality, and feasibility of the proposed project's EWD models and plans. Reviewers will therefore evaluate the extent to which the proposal's EWD plan:

(1) Includes rational and feasible targets, milestones, and metrics (e.g., students trained, graduated, and hired), appropriate to developing a diverse and skilled workforce and hiring, including by specific industry partners, into good jobs;
(2) Provides evidence of alignment with U.S. industry needs, such as demonstrated linkages between the skills to be developed and in-demand high-quality jobs or to industry-recognized curriculum, credentials, or certifications; and
(3) Encourages participation by underserved communities.

Relevant application materials include, but are not necessarily limited to, the **Impact Statement**, **Broader Impacts Statement**; and **Education and Workforce Development Plan.**

5.4 FULL APPLICATION SELECTION FACTORS

The selection factors for the full application in this competition are:

(1) Merit Review. Results of the merit reviewers' evaluations, including technical comments, and the evaluation panel's evaluations and adjectival rankings;
(2) Relevance to Program and Mission. Alignment with the objectives of this NOFO as well as the mission, goals, and priorities of the CHIPS R&D, which may include considerations related to research security, domestic production, and domestic control of intellectual property;
(3) Funding. The amount available to be awarded under this NOFO is subject to the availability of funds and applications received. CHIPS R&D reserves the right to make no awards under this NOFO;
(4) Non-Duplication. The degree to which the proposed project duplicates other projects funded by NIST or other Federal sources;
(5) Diversity of Projects and Participants. The degree to which the proposed team and project provides for a diversity of proposed project topics, regional diversity, and institutional diversity (including small and medium enterprises, universities, nonprofit research organizations, etc.) in the overall CHIPS R&D portfolio; and
(6) Broader Impacts and Workforce Development. The potential for the proposed project to contribute to broader U.S. research, development, innovation, manufacturing, education, workforce development, and regional economic development goals — including plans for broader impact consistent with Section 1.7 of this NOFO.

5.5 REVIEW AND SELECTION PROCESS

Proposals, reports, documents, and other information related to applications submitted to CHIPS R&D and/or relating to awards issued by CHIPS R&D will be reviewed and considered by Federal employees or non-Federal personnel who have entered into conflict of interest and confidentiality agreements covering such information, as applicable.

5.5.1 Initial Review of Applications

Concept papers and full applications received by the respective deadlines will be reviewed to determine eligibility, completeness, and responsiveness to this NOFO and stated program objectives. Concept papers and full applications determined to be ineligible, incomplete, and/or nonresponsive may be eliminated from further review. However, CHIPS R&D, in its sole discretion, may continue the review process for any concept paper or full application that is missing non-substantive information, the absence of which may easily be rectified during the review process.

Applicants are reminded that it is a crime to knowingly make false statements to a Federal agency. Misrepresentation of material facts may be the basis for denial of an application. Penalties upon conviction may include fine and imprisonment. For details, please refer to 18 U.S.C. § 1001.

5.5.2 Review of Concept Papers

Concept papers that are determined to be eligible, complete, and responsive to this NOFO will proceed for full reviews in accordance with the review and selection process set out below.

5.5.2.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.2.3) based on the evaluation criteria (see Section 5.1). While every concept paper will have at least three (3) reviewers, concept papers may have more than three (3) reviewers if specialized expertise is needed. During the review process, the reviewers may discuss concept papers with each other, but ratings will be determined on an individual basis, not a consensus. NIST may also complete a research security review of selected applications, contemporaneous with or after completion of the merit review.

5.5.2.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate expertise will conduct a panel review of the concept papers. The evaluation panel may contact applicants via e-mail to clarify the contents of a concept paper.

5.5.2.3 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each concept paper to the Selecting Official for further deliberation, considering:

- All concept paper materials;

- Results of the merit reviewers' evaluations, including written assessments;
- Any relevant publicly available information; and
- Any clarifying information obtained from the applicants.

The adjectival ratings that may be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, concept papers receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.2.4 Selection of Successful Concept Papers and Invitations to Submit Full Applications

The NIST Director or his or her designee will serve as the Selecting Official and will make final determinations regarding which concept papers to invite to submit full applications. The Selecting Official shall generally select the most meritorious concept papers for invitation based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select concept papers from a lower adjectival category based on one or more of the Selection Factors. The decisions of the Selecting Official regarding the selection of concept papers are final and may not be appealed. CHIPS R&D may publicly release or publish successful concept paper applicant names, as well as Executive Summaries and/or Quad Charts, including to facilitate re-teaming.

5.5.2.5 Feedback and Workshops

Prior to the deadline for submission of full applications, to ensure the quality of such applications, CHIPS R&D may, in its sole discretion, opt to provide feedback to applicants based on the findings of the merit reviewers and evaluation panels. CHIPS R&D may also, in its sole discretion, opt to administer additional workshops for applicants that are invited to submit full applications, including to support greater private sector teaming.

5.5.3 Review of Full Applications

Applications that are determined to be eligible, complete, and responsive will proceed for full reviews in accordance with the review and selection process set out below.

5.5.3.1 Merit Review

At least three (3) independent, objective reviewers, who may be Federal employees or non-Federal personnel, with appropriate expertise relating to the topics covered in this NOFO, will each provide a written evaluation and adjectival ratings (see Section 5.5.3.4 based on the

evaluation criteria (see Section 5.3). While every application will have at least three (3) reviewers, applications may have more than three (3) reviewers if specialized expertise is needed to evaluate an application. During the review process, the reviewers may discuss the applications with each other, but evaluations will be determined on an individual basis, not a consensus. NIST may also complete a research security review of selected applications, contemporaneous with or after completion of the merit review.

5.5.3.2 Evaluation Panel

Following the merit review, an evaluation panel consisting of CHIPS R&D staff and/or other Federal employees with the appropriate technical expertise will conduct a panel review of the ranked applications. The evaluation panel may contact applicants via e-mail to clarify contents of an application.

5.5.3.3 Pre-selection Interviews and Site Visits

At CHIPS R&D's discretion, applicants may be requested to participate in Pre-Selection Interviews and/or Site Visits during the evaluation panel phase, either at CHIPS R&D, the applicant's site, or a mutually agreed upon location, or via conference call or webinar. The interviews and site visits are intended to allow the applicant to provide clarifications on the contents of the application and to provide CHIPS R&D an opportunity to ask questions and collect relevant information. Information provided during the interview and/or site visit will contribute to CHIPS R&D's evaluation of the applications.

5.5.3.4 Adjectival Rating

The evaluation panel will provide a final adjectival rating and written evaluation of each full application to the Selecting Official for further deliberation, considering:

- All application materials;
- Results of the merit reviewers' evaluations, including written assessments;
- Any relevant publicly available information; and
- Any clarifying information obtained from the applicants.

The adjectival ratings that may be assigned are:

- Outstanding
- Very Good
- Average
- Deficient

For decision-making purposes, applications receiving the same adjectival rating will be considered to have an equivalent ranking.

5.5.3.5 Pre-Selection Discussion

Prior to any final award recommendations made by the Selecting Official, CHIPS R&D may request that applicants deemed most likely to receive an award to modify objectives, work plans, or team composition, as appropriate, or provide supplemental information. CHIPS R&D further reserves the right to negotiate budget costs with applicants deemed most likely to receive an award, which may include requesting that an applicant remove certain costs. Any request made to an applicant for any modifications to its application does not constitute a commitment by CHIPS R&D to make an award to the applicant.

5.5.3.6 Selection

The NIST Director or his or her designee will serve as the Selecting Official and will make final award recommendations to the NIST Agreements Officer. The Selecting Official shall generally select and recommend the most meritorious applications for an award based upon the adjectival ratings and one or more of the Selection Factors. The Selecting Official retains the discretion to select and recommend an application from a lower adjectival category based on one or more of the Selection Factors.

CHIPS R&D reserves the right to reject an application where information is uncovered that raises a reasonable doubt as to the responsibility of the applicant. CHIPS R&D may select some, all, or none of the applications, or part(s) of any application. The final approval of selected applications and issuance of awards will be by the NIST Agreements Officer. The award decisions of the NIST Agreements Officer are final and may not be appealed.

5.5.3.7 Federal Awarding Agency Review of Risk Posed by Applicants

To inform the review by the Selecting Official, NIST will also conduct the research security review described in Section 2.5.6 and the results will be provided to the Selecting Official. Applicants with proposals that have been assessed as having medium or high risk may be given an opportunity to mitigate the risk, as described in Section 2.5.8.

After applications are proposed for funding by the Selecting Official, the NIST Financial Assistance Agreements Management Office (FAAMO) performs pre-award risk assessments, which may include a review of the financial stability of an applicant, the quality of the applicant's management systems, the history of performance, and/or the applicant's ability to effectively implement statutory, regulatory, or other requirements imposed on award recipients.

In addition, prior to making an award where the total Federal share is expected to exceed the simplified acquisition threshold (currently $250,000), NIST FAAMO will review and consider the publicly available Responsibility/Qualification records about that applicant available in SAM.gov (formerly available via the Federal Awardee Performance and Integrity Information System (FAPIIS)). An applicant may, at its discretion, review and comment on information about itself previously entered into SAM.gov by a Federal awarding agency. As part of its review of risk posed by applicants, NIST FAAMO will consider any comments made by the applicant in SAM.gov in making its determination about the applicant's integrity, business ethics, and record of performance under Federal awards. Upon completion of the pre-award risk

assessment, the NIST Agreements Officer will make a responsibility determination concerning whether the applicant is qualified to receive the subject award and, if so, whether appropriate specific conditions that correspond to the degree of risk posed by the applicant should be applied to an award.

5.6 ADDITIONAL INFORMATION

5.6.1 Safety

Safety is a top priority at NIST. Employees and affiliates of award recipients who conduct project work at NIST will be expected to be safety-conscious, to attend NIST safety training, and to comply with all NIST safety policies and procedures, and with all applicable terms of their guest research agreement.

5.6.2 Notification to Unsuccessful Applicants

Unsuccessful applicants will be notified by e-mail and will have the opportunity to receive a debriefing after this funding opportunity has officially closed. Applicants must request, within 10 business days of the e-mail notification, a debriefing from CHIPS R&D. CHIPS R&D will then work with the applicant in arranging a date and time for the debriefing.

5.6.3 Retention of Unsuccessful Applications

Unsuccessful applications will be retained in accordance with the General Record Schedule 1.2/021.

6 FEDERAL AWARD ADMINISTRATION INFORMATION

6.1 FEDERAL AWARD NOTICES

Successful applicants will receive an award package electronically from the NIST Agreements Officer.

6.2 ADMINISTRATIVE AND NATIONAL POLICY REQUIREMENTS

6.2.1 Terms and Conditions

The complete terms and conditions of each award will be contained in the award package signed by the NIST Agreements Officer.

6.2.1.1 NIST/CHIPS R&D Discretion

Awards under this program require significant ongoing involvement from CHIPS R&D staff, to provide NIST the flexibility to alter the course of the project in real-time and to meet the

overarching program goals. This will generally include collaboration with the recipient organization in developing and implementing the approved scope of work.

6.2.1.2 Management Systems and Procedures

Recipient organizations are expected to have systems, policies, and procedures in place by which they manage funds and activities. Recipients may use their existing systems to manage Federal award funds and activities as long as they are consistently applied regardless of the source of funds and across their business functions. To ensure that an organization is committed to compliance, recipient organizations are expected to have in place written policies and procedures that provide for: clearly delineated roles and responsibilities for their organization's staff, both programmatic and administrative; training; management controls and other internal controls; performance assessment; administrative simplifications; and information sharing.

6.2.1.3 Financial Management System Standards

Recipients must have in place accounting and internal control systems that provide for appropriate monitoring of other transaction accounts to ensure that obligations and expenditures are congruent with programmatic needs and are reasonable, allocable, and allowable. In addition, the systems must be able to identify unobligated balances, accelerated expenditures, inappropriate cost transfers, and other inappropriate obligation and expenditure of funds, and recipients must notify CHIPS R&D when problems are identified. A recipient's failure to establish adequate control systems constitutes a material violation of the terms of the award.

6.2.2 Funding Availability and Limitation of Liability

Funding for the program described in this NOFO is contingent upon the availability of appropriations. The U.S. Department of Commerce or NIST will not be responsible for application preparation costs, including but not limited to if this program fails to receive funding or is cancelled because of agency priorities. Publication of this NOFO does not oblige the U.S. Department of Commerce or NIST to award any specific project or to obligate any available funds.

6.2.3 Collaborations with CHIPS R&D and Other Federal Agencies

CHIPS R&D employees may not participate in the preparation of any application in response to this funding opportunity. After award, the team is expected to interact with CHIPS R&D and with Federal government organizations and FFRDCs, as appropriate and consistent with their respective missions, objectives, and operational structures.

The award recipient is encouraged to collaborate with Federal entities to support the program goals and to ensure that the Federal investment in this team can be leveraged to the extent appropriate for national priorities.

If an applicant proposes collaboration with NIST, the statement of work must include a statement of this intention, a description of the collaboration, and prominently identify the NIST employee(s) involved, if known. Any collaboration by a NIST employee must be approved by appropriate NIST management and is at the sole discretion of NIST. Prior to beginning the merit review process, NIST will verify the approval of the proposed collaboration. Any unapproved collaboration will be stricken from the application prior to the merit review. Any collaboration with an identified NIST employee that is approved by appropriate NIST management will not make an application more or less favorable in the competitive process.

6.2.4 Use of Federal Government-Owned Intellectual Property

If the applicant anticipates using any Federal government-owned intellectual property, in the custody of CHIPS R&D or another Federal agency, to carry out the work proposed, the applicant must clearly identify such intellectual property in its proposal. This information will be used to ensure that no Federal employee involved in the development of the intellectual property will participate in the review process for that competition. In addition, if the applicant intends to use the Federal Government-owned intellectual property, the applicant must comply with all statutes and regulations governing the licensing of Federal government patents and inventions, described in 35 U.S.C. § 200-212, 37 C.F.R. Part 401, 2 C.F.R. § 200.315. Questions about these requirements may be directed to the Chief Counsel for NIST at (301) 975-2803 and via e-mail at nistcounsel@nist.gov.

Any use of Federal government-owned intellectual property by a recipient of an award under this announcement is at the sole discretion of the Federal government and will need to be negotiated on a case-by-case basis by the recipient and the Federal agency having custody of the intellectual property if a project is deemed meritorious. The applicant must indicate within the statement of work whether it already has a license to use such intellectual property or whether it intends to seek a license from the applicable Federal agency.

If any inventions made in whole or in part by a NIST employee arise in the course of an award made pursuant to this NOFO, the United States Government may retain its ownership rights in any such invention.

Licensing or other disposition of the Federal government's rights in such inventions will be determined solely by the Federal government, through CHIPS R&D as custodian of such inventions and include the possibility of the Federal government putting the intellectual property into the public domain.

6.2.5 Export Controls

Some activities may require access to export-controlled items and therefore be subject to export control laws and regulations. If an applicant is selected for award, the applicant and all subrecipients agree to comply with United States export laws and regulations, including, but not limited to, the International Traffic in Arms Regulations and the U.S. Department of Commerce Export Administration Regulations. Under no circumstances may foreign entities (organizations,

companies, or persons) obtain access to export-controlled items unless proper procedures have been satisfied and such access is authorized pursuant to law or regulation. If involvement of foreign entities is approved by CHIPS R&D, recipients must develop measures to properly protect export-controlled information, as appropriate. Approval of foreign entity involvement by CHIPS R&D does not constitute approval or waiver of any export licensing requirements that may apply.

Regarding any project-funded innovation (which may include software), recipients remain responsible for complying with all applicable laws, regulations, and policies governing intellectual property rights, licensing, and export control.

CHIPS R&D reserves the right to seek and consider additional information, including from applicants regarding their current compliance with export laws and regulations, or any pending investigations thereof, at any point in the selection process.

6.3 REPORTING

6.3.1 Reporting Requirements

The following reporting requirements apply to awards made in this program:

6.3.1.1 Financial Reports

Each award recipient will be required to submit financial reports. Financial reporting requirements will be outlined in the terms and conditions of the award.

6.3.1.2 Research Performance Monitoring and Reporting

Award recipients will be required to submit quarterly progress reports within 30 days of the close of each reporting period. CHIPS R&D expects the recipient to include similar content to that requested in the Research Performance Progress Report (see 2 C.F.R. § 200.329). However, CHIPS R&D may approve the use of a different format at the request of the recipient. Detailed progress reporting requirements will be outlined in the terms and conditions of the award.

A final consolidated report shall be submitted within 120 days after the expiration date of the award. The recipient is required to submit publication citation information, links to publicly available data, and other public outputs as soon as they become available.

In addition to the formal quarterly progress reports, the award recipient will be expected to meet quarterly with the Federal Program Officer to discuss operational, technical, and strategic plans. It is expected that the recipient will additionally establish regular and ongoing cadence of informal communication with the Federal program team to ensure timely awareness of issues and achievements.

The recipient also will be expected to report progress against specific NIST-issued activity metrics at the end of each phase period. NIST will work with the recipient in the start-up phase of the award to implement activity metrics.

Information submitted in the course of applying for funding under this program or provided in the course of its grant management activities, will be subject to analysis and evaluation for official Government or statistical purposes, including but not limited to assessing performance and evaluating program outcomes.

6.3.1.3 Patent and Property Reports

In accordance with the terms and conditions governing the award, the recipient may need to submit property and patent reports. The award recipient is required to notify CHIPS R&D of any patents or other intellectual property issuing from work performed within this award. CHIPS R&D requires periodic reporting on the utilization or efforts at obtaining utilization that are being made by the recipient or its licensees or assignees, *provided that* any such information, as well as any information on utilization or efforts at obtaining utilization shall be treated by the Federal agency as commercial and financial information obtained from a person and privileged, confidential, and not subject to disclosure.

6.3.1.4 Recipient Integrity and Performance Matters

In accordance with section 872 of Public Law 110-417 (as amended; see 41 U.S.C. § 2313), if the total value of a recipient's currently active grants, cooperative agreements, and procurement contracts from all Federal awarding agencies exceeds $10,000,000 for any period of time during the period of performance of an award made under this NOFO, then the recipient shall be subject to maintaining the currency of information reported to SAM that is made available in FAPIIS about certain civil, criminal, or administrative proceedings involving the recipient.

6.3.2 Audit Requirements

Any recipient that expends Federal awards of $1,000,000 or more in the recipient's fiscal year must conduct a single or program specific audit similar to the requirements set out in the 2 C.F.R. Part 200, Subpart F. Additionally, unless otherwise specified in the terms and conditions of the award, entities that are not subject to Subpart F of 2 C.F.R. Part 200 (e.g., for-profit commercial entities) that expend $1,000,000 or more in DOC funds during their fiscal year must submit to the assigned NIST Agreements Officer either(1) a financial related audit of each DOC award or subaward in accordance with Generally Accepted Government Auditing Standards or (2) a project specific audit for each award or subaward with similar content to that requested in 2 C.F.R. § 200.507. Applicants are reminded that CHIPS R&D, the U.S. Department of Commerce Office of Inspector General, or another authorized Federal agency may conduct an audit of an award at any time.

6.3.3 Federal Funding and Accountability Transparency Act of 2006

In accordance with 2 C.F.R. Part 170, all recipients of a Federal award made on or after October 1, 2010, are required to comply with reporting requirements under the Federal Funding Accountability and Transparency Act of 2006 (Public Law No. 109-282). In general, all recipients are responsible for reporting sub-awards of $25,000 or more. In addition, recipients that meet certain criteria are responsible for reporting executive compensation. Applicants must ensure they have the necessary processes and systems in place to comply with the reporting requirements should they receive funding. Also see the *Federal Register* notice published on September 14, 2010, at 75 FR 55663.

7 AGENCY CONTACTS

Applicants must submit any questions pertaining to this funding opportunity in writing to the following points of contact, as appropriate:

Subject Area	Point of Contact
Programmatic and Technical Questions	E-mail: research@chips.gov with "2025-NIST-CHIPS-AIAE-Sustainability-01" in the subject line
Technical Assistance with Grants.gov Submissions	www.grants.gov Phone: 800-518-4726 E-mail: support@grants.gov
Agreement Management Inquiries	Lisa Ko E-mail: NOFO@nist.gov with "2025-NIST-CHIPS-AIAE-Sustainability-01 Questions" in the subject line

8 OTHER INFORMATION

8.1 PERSONAL AND BUSINESS INFORMATION

The applicant acknowledges and understands that information and data contained in applications for other transaction agreements, as well as information and data contained in financial, performance and other reports submitted by applicants, may be used by CHIPS R&D in conducting reviews and evaluations of its financial assistance programs. For this purpose, applicant information and data may be accessed, reviewed, and evaluated by U.S. Department of Commerce employees, other Federal employees, and also by Federal agents and contractors, and/or by non-Federal personnel, who enter into conflict of interest and confidentiality agreements covering the use of such information as appropriate. As may be provided in the terms and conditions of a specific other transaction agreement, applicants are expected to support program reviews and evaluations by submitting required financial and performance information and data in an accurate and timely manner, and by cooperating with U.S. Department of Commerce and external program evaluators. Applicants must safeguard protected personally identifiable information and other confidential or sensitive personal or business information created or obtained in connection with a U.S. Department of Commerce financial assistance

award consistent with information security requirements under applicable standards, this NOFO, and the terms and conditions of the award.

In addition, U.S. Department of Commerce regulations implementing the Freedom of Information Act (FOIA), 5 U.S.C. § 552, are found at 15 C.F.R. Part 4, Disclosure of Government Information. These regulations set forth rules for the U.S. Department of Commerce regarding making requested materials, information, and records publicly available under the FOIA. Applications submitted in response to this Federal Funding Opportunity may be subject to requests for release under the FOIA. If an application contains information or data that the applicant deems to be confidential commercial information that should be exempt from disclosure under FOIA, that information should be marked as "Proprietary," "Sensitive Business Information," or similar markings as specified in Section 4.4.2 of this NOFO. In accordance with 15 C.F.R. § 4.9, CHIPS R&D and the U.S. Department of Commerce will protect from disclosure confidential business information contained in other transaction applications and other documentation provided by applicants to the extent permitted by law.

8.2 PUBLIC WEBSITE

CHIPS R&D has a public website that includes a Frequently Asked Questions page and other information pertaining to this funding opportunity. Any amendments to this NOFO will be announced through Grants.gov.

Applicants must submit all questions pertaining to this funding opportunity in writing to research@chips.gov with "2025-NIST-CHIPS-AIAE-Sustainability-01 Questions" in the subject line.

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